

COMPAL CONFIDENTIAL

MODEL NAME : FDI45, FDI55

PCB NO : DA600273000

BOM P/N : 431AII31L51

ICL-U+MEC1418

2019-07-31

REV : 1.0 (A00)

@ : Un-pop Component

N3@/V3@: : Inspiron (fTPM)/Vostro (HW TPM)

ICL@/ : ICL-U

BASE@/PREM@ : Pentium,Celeron/i3,i5,i7

EC@ : EC Support

JP@/PJP@ : JUMP

100@/1000@: Lan

NOI2CTCH@/I2CTCH@: USB touch / I2C touch

EMI@/ESD@/RF@ : EMI, ESD and RF Component

@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component

CMC@ : XDP Component

CONN@ : Connector Component

KBBL@ : KB Backlight

750_CTPM@:750 and china TPM

ST_CTPM@:ST and china TPM

CTPM@:China TPM

FFS@ : Free Fall Sensor

TYPEC@ : TypeC

TYPEC@EMI@/TYPEC@ESD@: EMI, ESD ,TypeC Component

PCB@/PCB_R1@/PCB_R3_G@/PCB_R3_T@/PCB_R3_H@/PCB_R3_TM@: PCB MB

CPU R1

UC1 QS_I3@
FJ8068904312504 QSQW
Part Number = SA0000CTD0L
S IC A31 FJ8068904312504 QSQW D1 1.2G S

UC1 QS_I5@
FJ8068904368700 QSW3
Part Number = SA0000CUQ0L
S IC A31 FJ8068904368700 QSW3 D1 1G S

UC1 QS_I7@
FJ8068904310403 QSQS
Part Number = SA0000CT60L
S IC A31 FJ8068904310403 QSQS D1 1.3G S

CPU R3

UC1 PRO_I3@
FJ8068904312504 SRG0S
Part Number = SA0000CTD2L
S IC FJ8068904312504 SRG0S D1 1.2G A31 !

UC1 PRO_I5@
FJ8068904312402 SRGKL
Part Number = SA0000CTB2L
S IC FJ8068904312402 SRGKL D1 1G A31 !

UC1 PRO_I7@
FJ8068904310403 SRG0N
Part Number = SA0000CT62L
S IC FJ8068904310403 SRG0N D1 1.3G A31 !

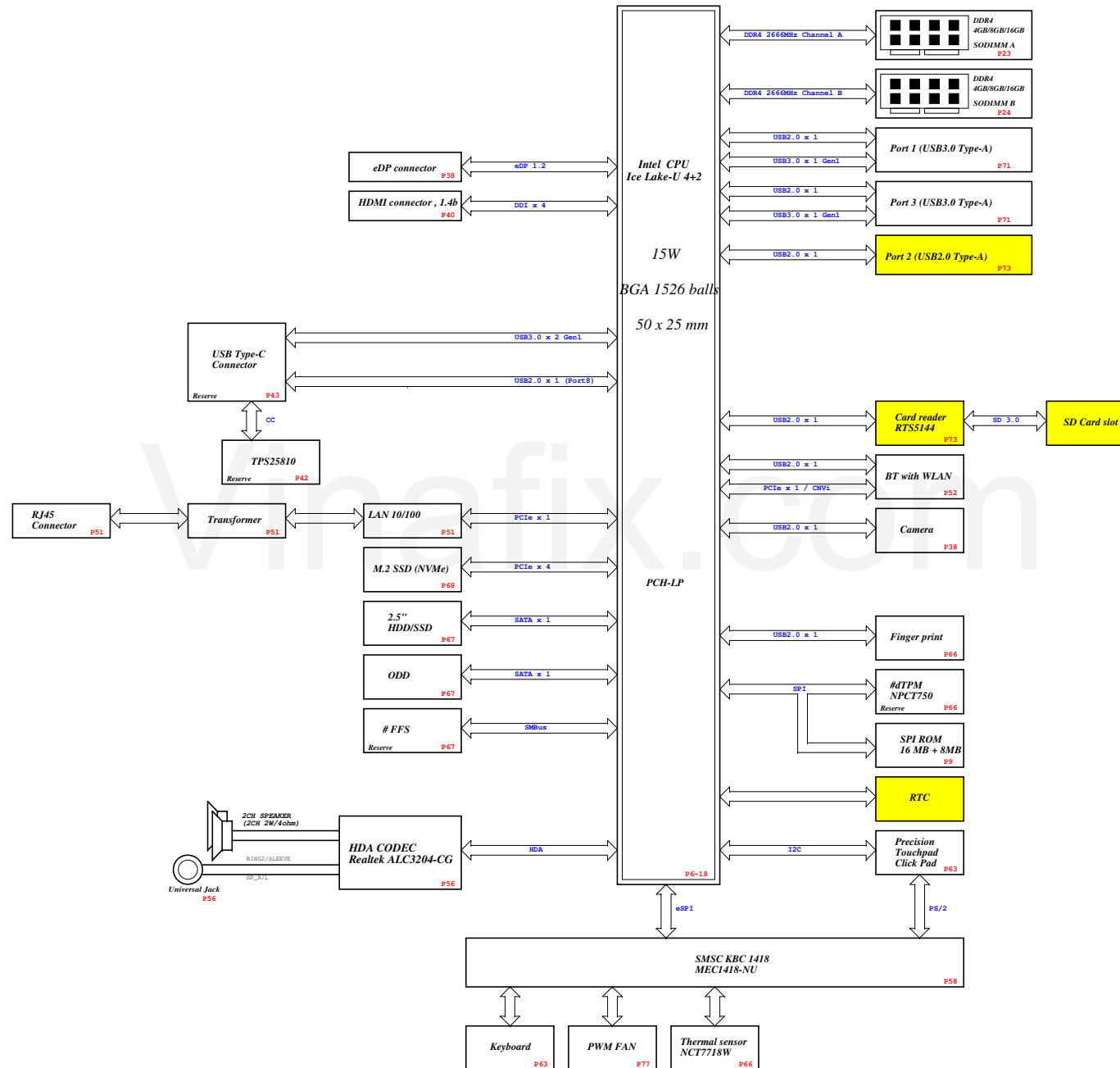
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PWB: 9HTP8

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Block Diagram



POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

Voltage Rails

Power Plane	Description	S0	S3	S4/S5	G3
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A	N/A
+RTC_SOC	RTC power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*	OFF
+5VALW	System +5V always on power rail	ON	ON	ON*	OFF
+3VALW	System +3V always on power rail	ON	ON	ON*	OFF
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*	OFF
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+2.5V_MEM	DDR4 +2.5v power rail	ON	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	ON	ON	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF	OFF
VCCPLL	+1.05 VCCPLL power rail	ON	ON	ON	OFF
+VCC_IN	Core voltage for CPU	ON	OFF	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	OFF
+3VALW_DSW	+19VB to D5W power rail for suspend power	ON	ON	ON	OFF
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*	OFF
+5VS	System +5VS power rail	ON	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF	OFF
+1.35V_MEM_GFX	+1.35V power rail for GPU	ON	OFF	OFF	OFF
+3VGS	+3V power rail for GPU	ON	OFF	OFF	OFF
+1.8VGS	+1.8V power rail for GPU	ON	OFF	OFF	OFF
+0.35VSDGPU	+0.95V power rail for GPU	ON	OFF	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

零件表: Wu, Fakir <eddie.wu@intel.com>
设计者: Chiu, AlexCL (TPE); Chen, Johnny (TPE); Hong, Henry (TPE); Chang, Jay S.; Liu, Joe (TPE); Lai, Carol (TPE); Kenny, Lu@dellem.com
副主: Chen, AlexCL (TPE); Chang, Gary.; Hsiao, Jimmy
主图: RE: ICL N3V3 MLK High Power Consumption on VCCIN_AUX Under S3/S5

Hi David,
VCCIN_AUX only down to 0V while SLP_S0# is asserted.
On S3 mode, it only can down to 1.1V. Thanks.

Best Regards,
Eddie Wu +886-2-66221110

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 port3, IO/B
4	Touch screen
5	Finger printer
6	CCD
7	Card reader , IO/B
8	TypeC-C
9	Reserved
10	BT

Board ID & Model ID Table

		N3V3_MLK-CML PCBA (EC-A ver)		N3V3_MLK-ICL PCBA (EC-B ver - ISL9522 / EC-C ver - ISL9538 + CGG5C)	
		Model_ID (RE4 PD-100K)	Board_ID (RE2 PD-100K)	Model_ID (RE4 PD-100K)	Board_ID (RE2 PD-100K)
SBDR (N3/V3)	UMA+N/A	RE3 PU-10K		RE3 PU-10K	
	UMA+TypeC (Data Only)	RE3 PU-17.8K	RE1 PU-10K-EVT	RE3 PU-17.8K	RE1 PU-10K-EVT
NBDR (N5/V5)	UMA+N/A	RE3 PU-27.0K	RE1 PU-17.8K-DVT1	RE3 PU-27.0K	RE1 PU-17.8K-DVT1
	UMA+TypeC (Data Only)	RE3 PU-37.4K	RE1 PU-27.0K-Reserve	RE3 PU-37.4K	RE1 PU-27.0K-Reserve
SBDR (N3/V3)	DSC+N/A	RE3 PU-49.9K	RE1 PU-37.4K-DVT2	RE3 PU-49.9K	RE1 PU-37.4K-DVT2
	DSC+TypeC (Data Only)	RE3 PU-64.9K	RE1 PU-49.9K-Reserve	RE3 PU-64.9K	RE1 PU-49.9K-Reserve
NBDR (N5/V5)	DSC+N/A	RE3 PU-82.5K	RE1 PU-64.9K-Pilot	RE3 PU-82.5K	RE1 PU-64.9K-Pilot
	DSC+TypeC (Data Only)	RE3 PU-107K	RE1 PU-82.5K-Reserve	RE3 PU-107K	RE1 PU-82.5K-Reserve

Table 11-23. System with M3 State Supported

Rails	SKUs	S0/M0 ³	C10 ²	S0ix/M-off ⁴	S3/M3	S3/M-off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3 ¹
RTC Well	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
3.3V_DSW	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V1.8A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V1.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VNN_BYPASS	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V1.05_BYPASS	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M ⁵	All	ON	ON	OFF	ON ¹⁰	OFF	ON ¹⁰	OFF	OFF	No Power
V1.8M ⁵	All	ON	ON	OFF	ON ¹⁰	OFF	ON ¹⁰	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST ^{12, 15}	All	ON	ON	ON	ON ¹³	ON ¹³	ON	OFF ⁶	OFF	No Power
TCSS/AGSH	All	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCSTG	All	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCPLL	All	ON	ON	ON	ON ¹³	ON ¹³	ON	ON	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	No Power
VCCPLL_OC ¹²	All	ON	ON	OFF ¹¹	ON ^{8, 13}	ON ^{8, 13}	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON ¹¹	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON ¹¹	ON	OFF ¹⁴	ON	OFF ¹⁴	OFF	No Power

Note : VCCIN_AUX only down to 0V while SLP_S0# is asserted. On S3 mode, it only can down to 1.1V.

USB3.0	PCIe	SATA	DESTINATION
USB3.0-1	PCIe-1		USB3.0 (MB)(Type-A)
USB3.0-2	PCIe-2		USB3.0 (MB)(Type-A)
USB3.0-3	PCIe-3		USB3.0 (Type-C)
USB3.0-4	PCIe-4		USB3.0 (Type-C)
USB3.0-5	PCIe-5		GPU
USB3.0-6	PCIe-6		GPU
	PCIe-7		GPU
	PCIe-8		GPU
	PCIe-9		LOM
	PCIe-10		WLAN
	PCIe-11	SATA-0	SATA HDD
	PCIe-12	SATA-1A	SATA ODD
	PCIe-13		NVME SSD
	PCIe-14		NVME SSD
	PCIe-15	SATA-1B	NVME SSD
	PCIe-16	SATA-2	NVME SSD

High Speed I/O (HSIO) Lane Multiplexing in ICL U PCH-LP

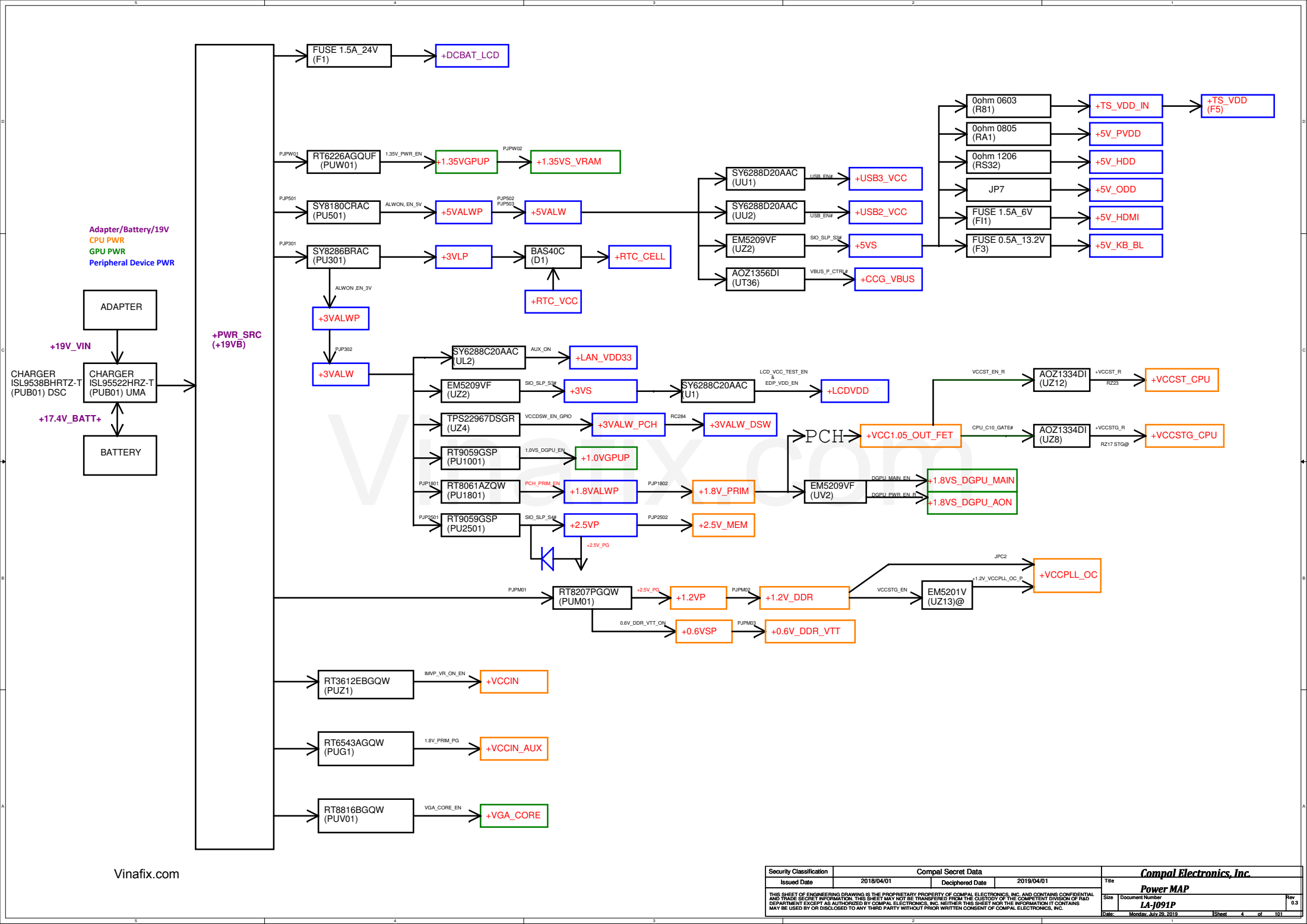
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16
	PCIe #1	PCIe #2	PCIe #3	PCIe #4	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16
PCIe# Backup Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

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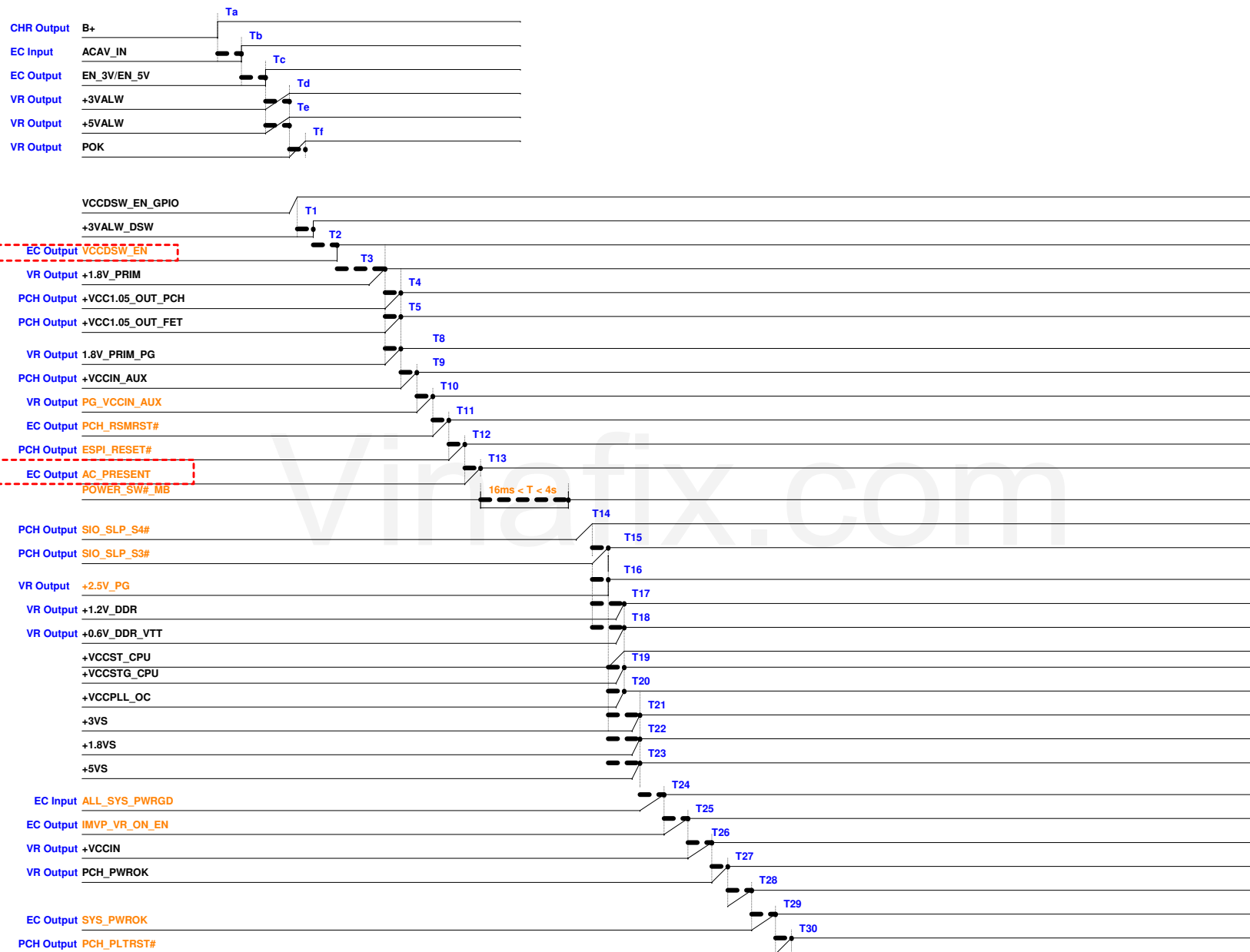
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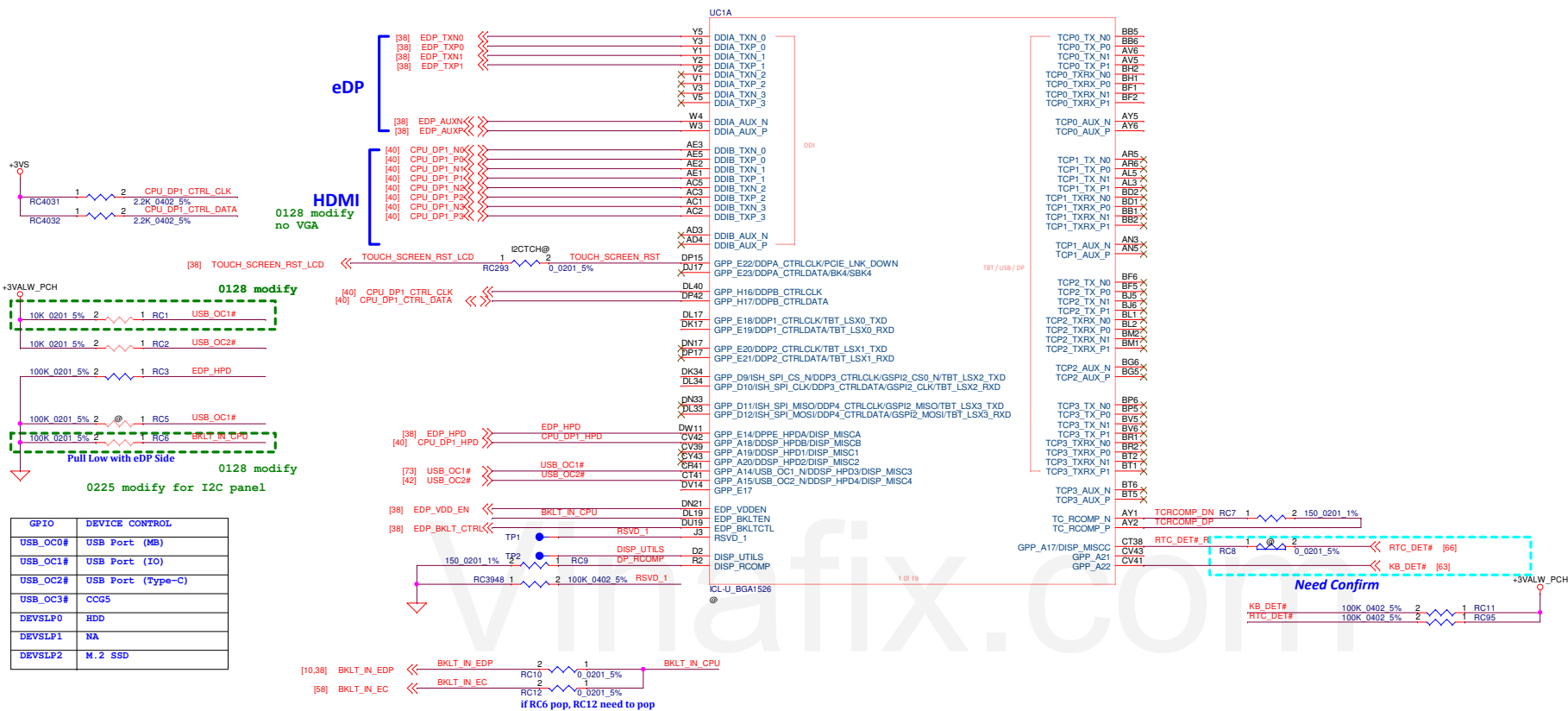
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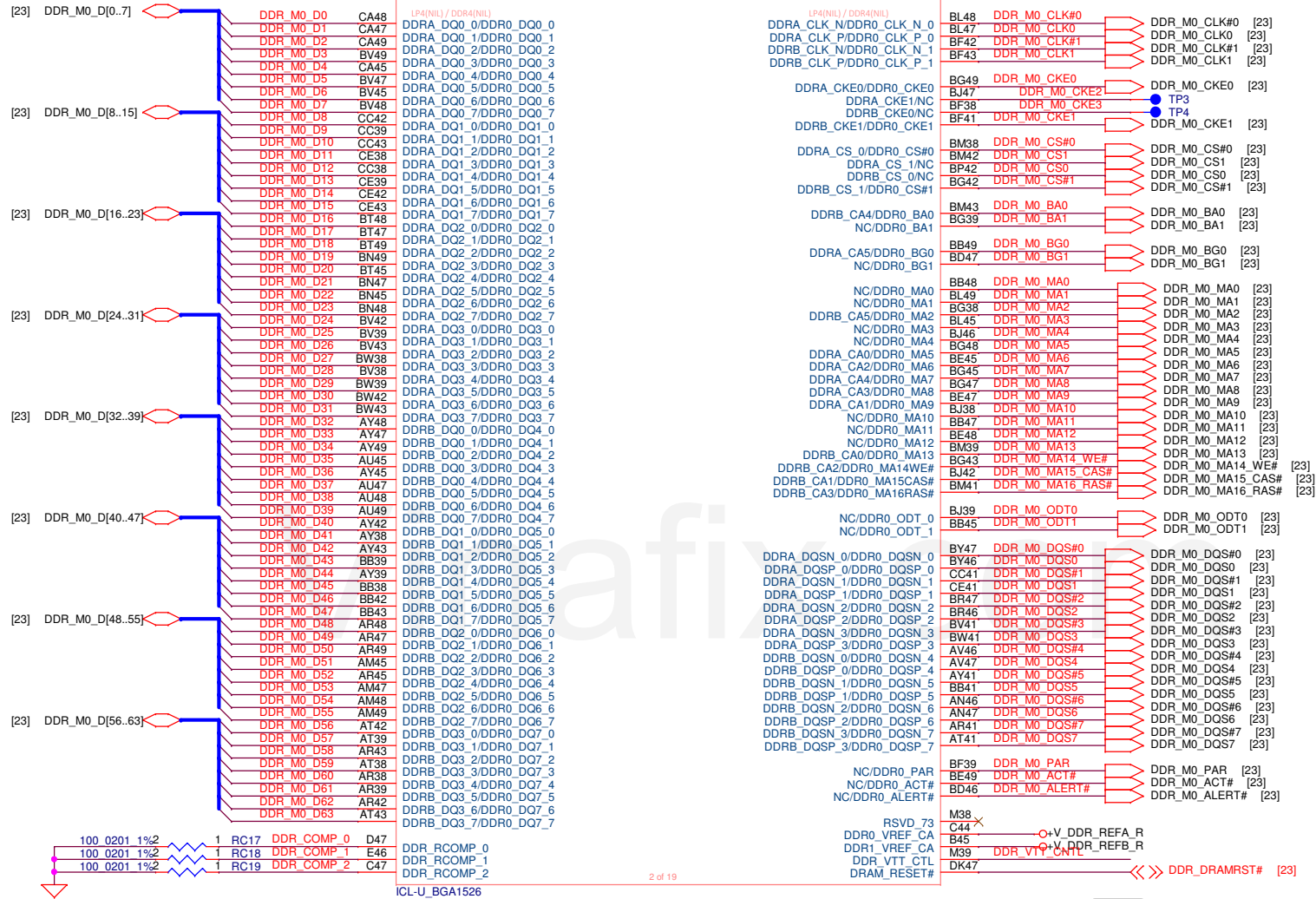


Power Up Sequence

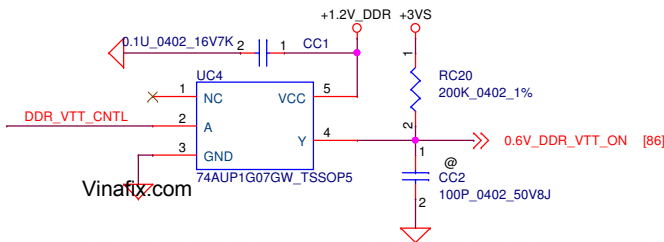




Main Function: CPU (2/13)

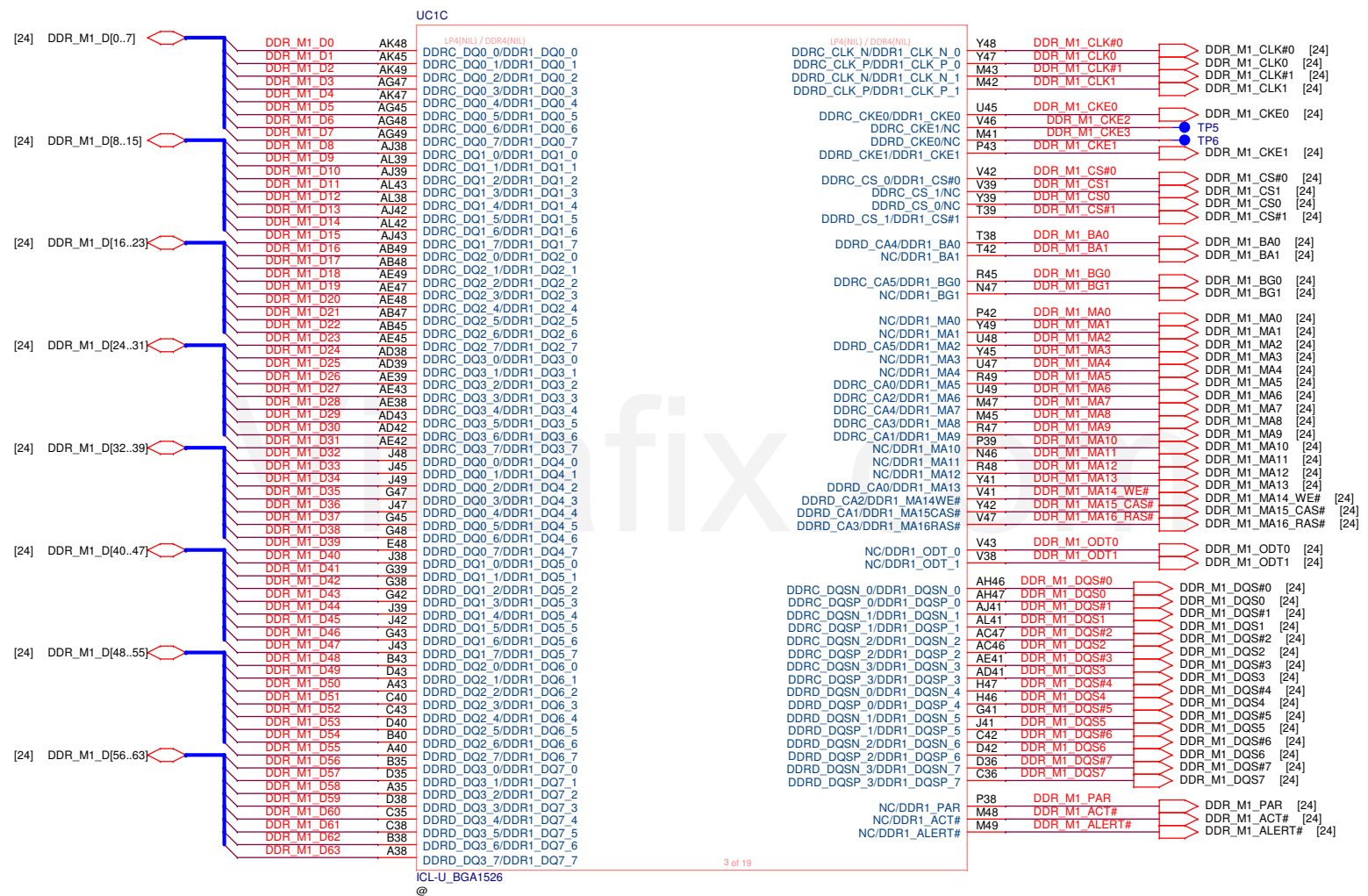


CAD Note:
Min trace width=20 mils, spacing of adjacent signal=20 mils



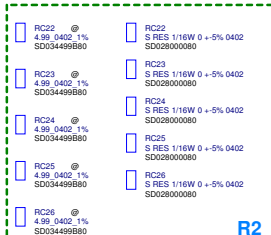
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Main Function: CPU(3/13)

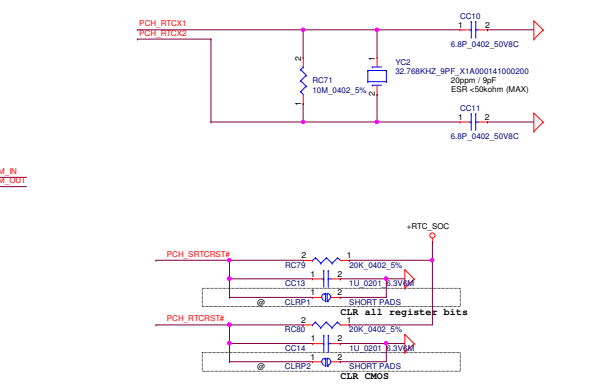
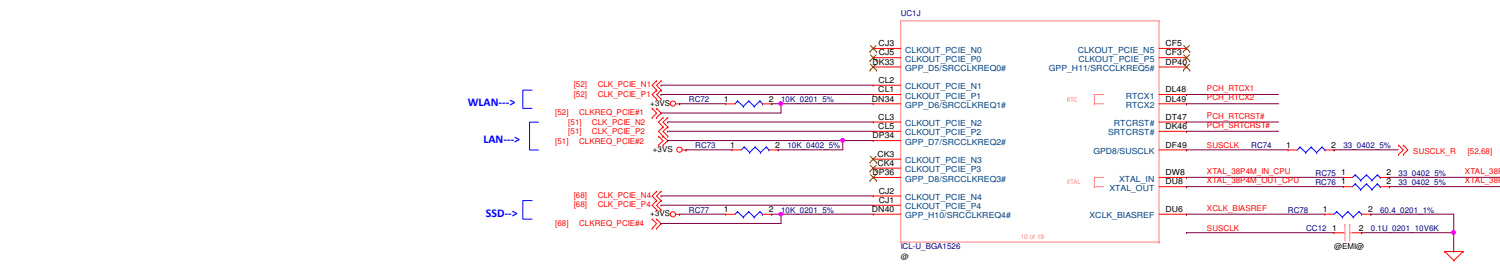
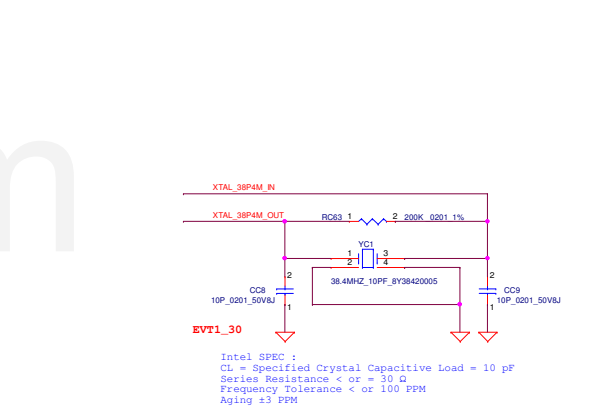
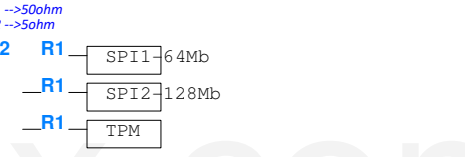
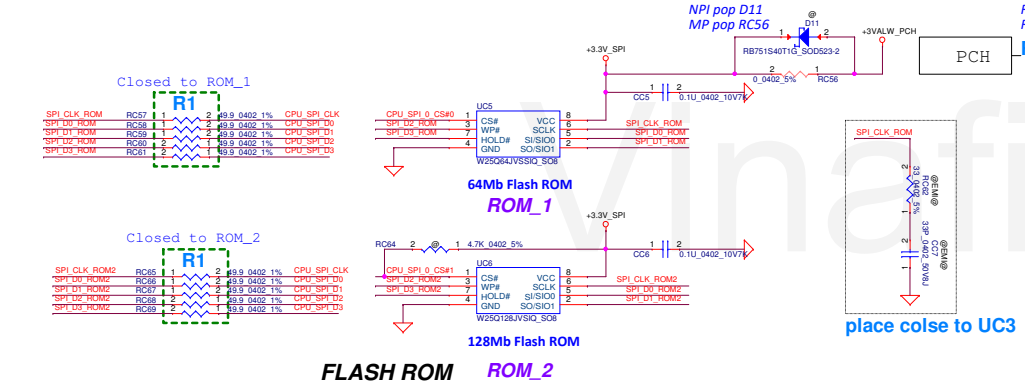
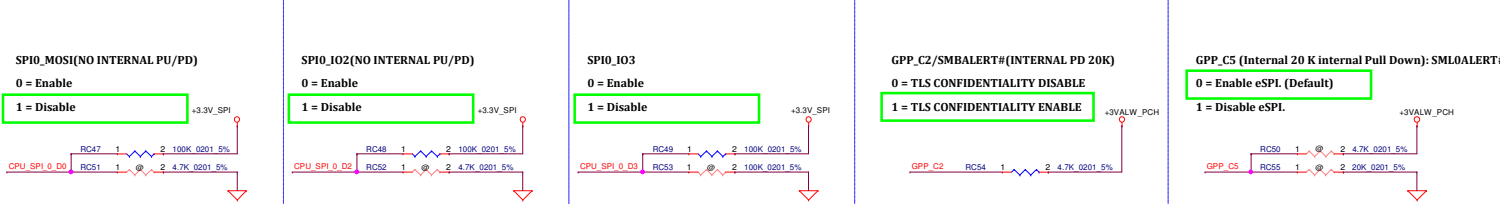


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Main Function: CPU (4/13)



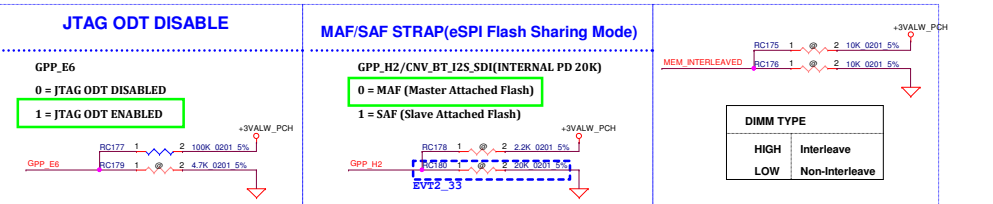
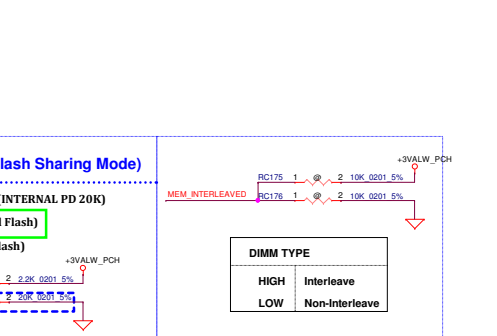
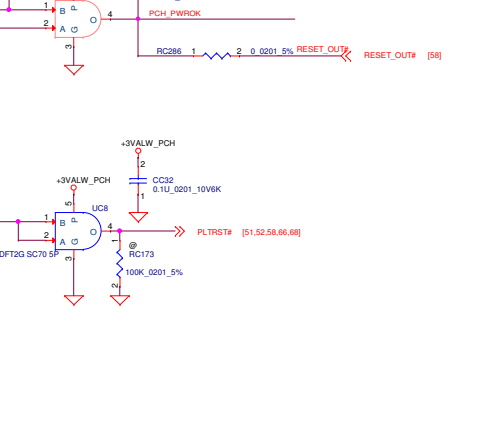
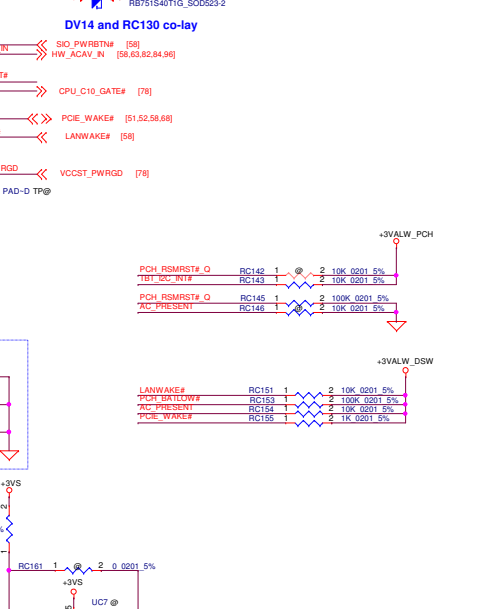
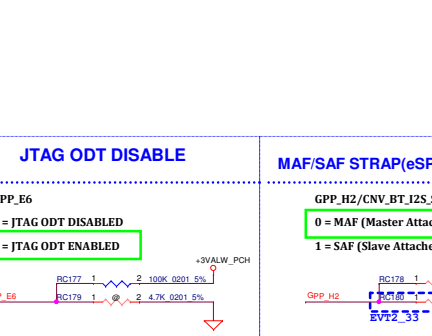
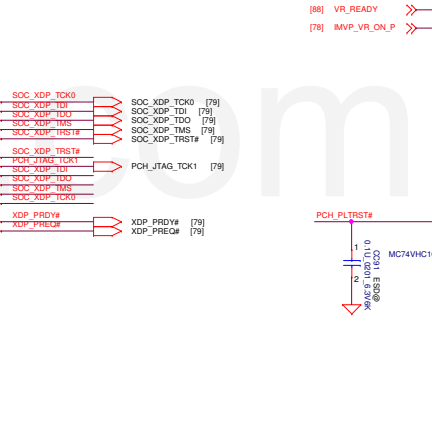
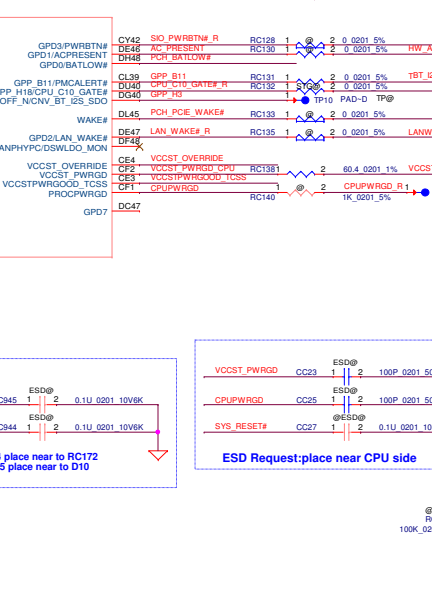
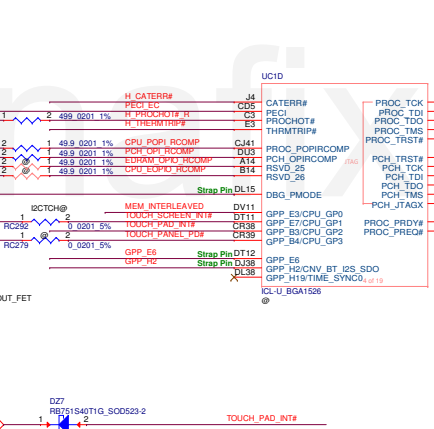
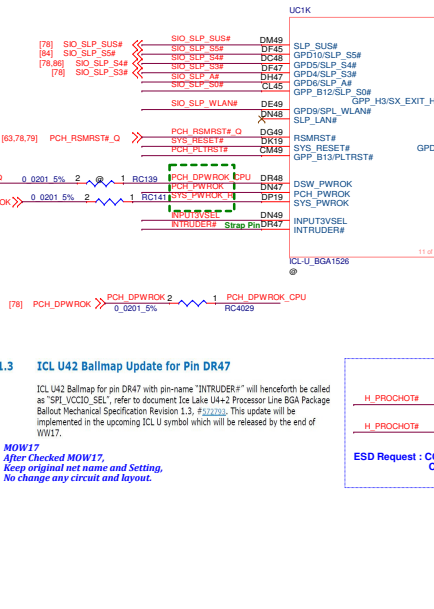
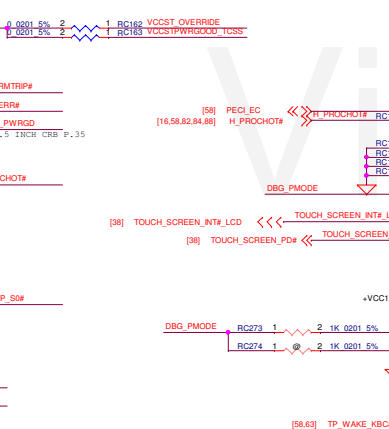
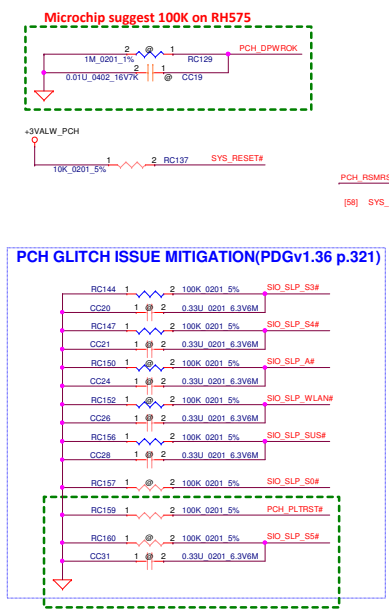
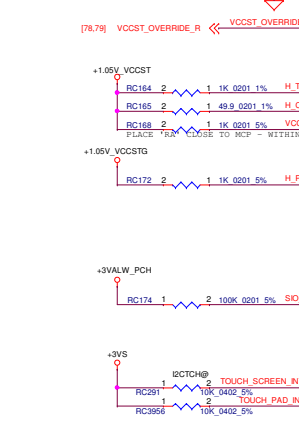
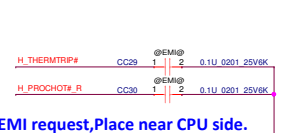
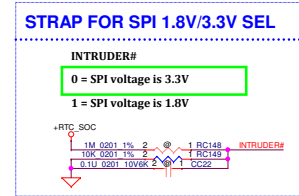
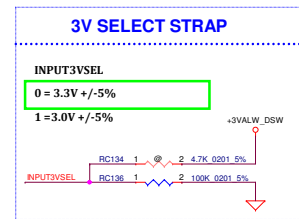
R2 Resistor should be 50 for 1.8V and 3.3V.
R2 to be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3. It is an optional to have R2 on the channel. It can be removed to reduce BOM cost.

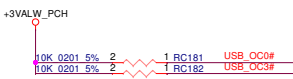
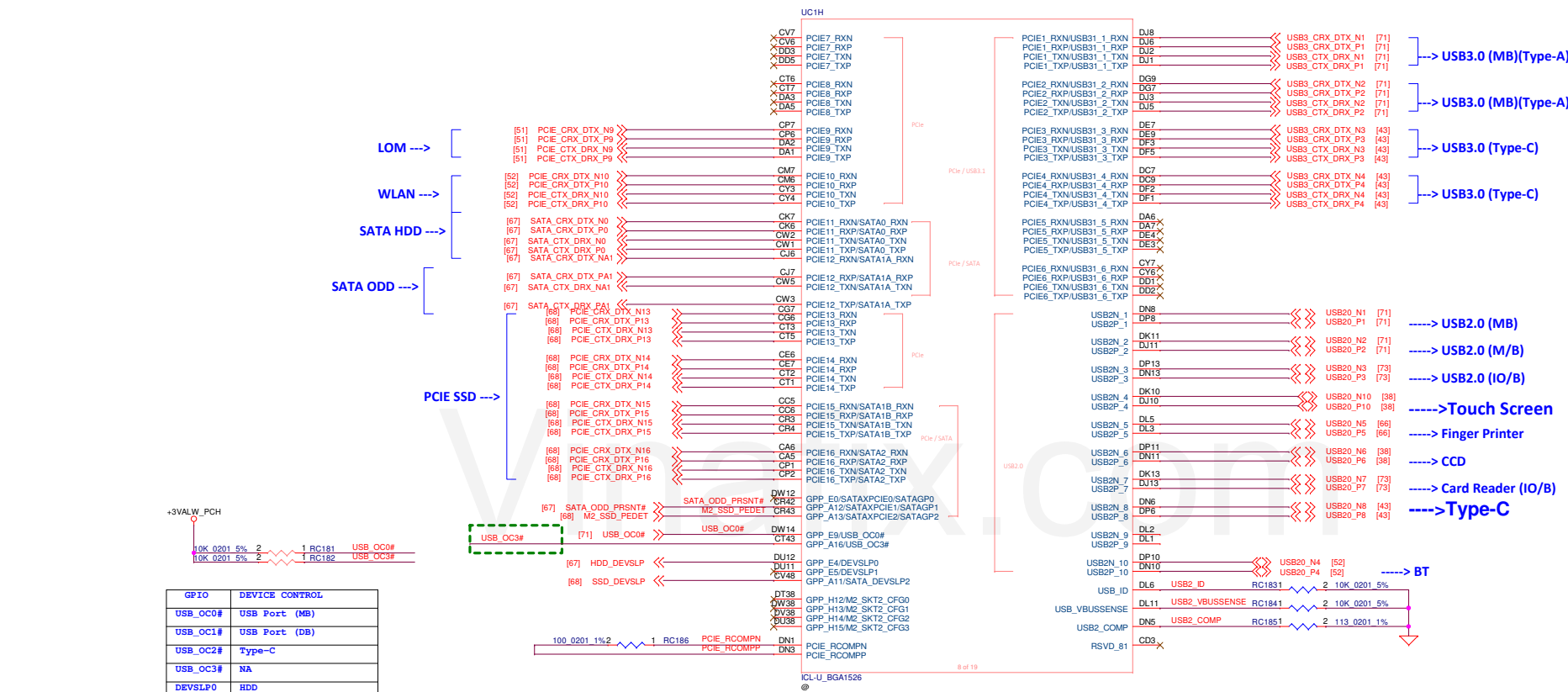


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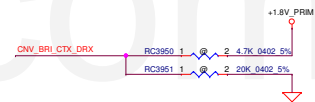


GPIO	DEVICE CONTROL
USB_OC0#	USB Port (MB)
USB_OC1#	USB Port (DB)
USB_OC2#	Type-C
USB_OC3#	NA
DEVSLP0	HDD
DEVSLP1	NA
DEVSLP2	M.2 SSD

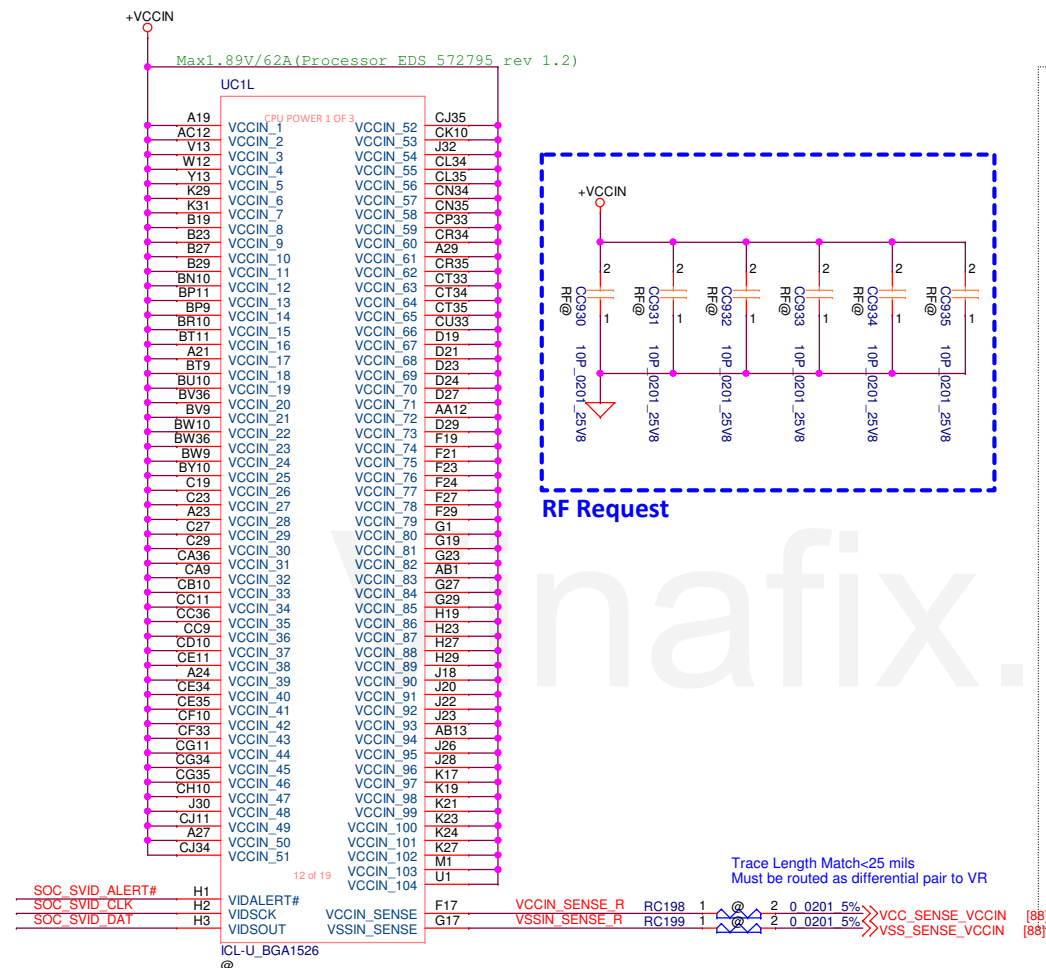


CNV_RGI_CTX_DRX
M.2 CNVi MODES
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
NO INTERNAL PU/PD

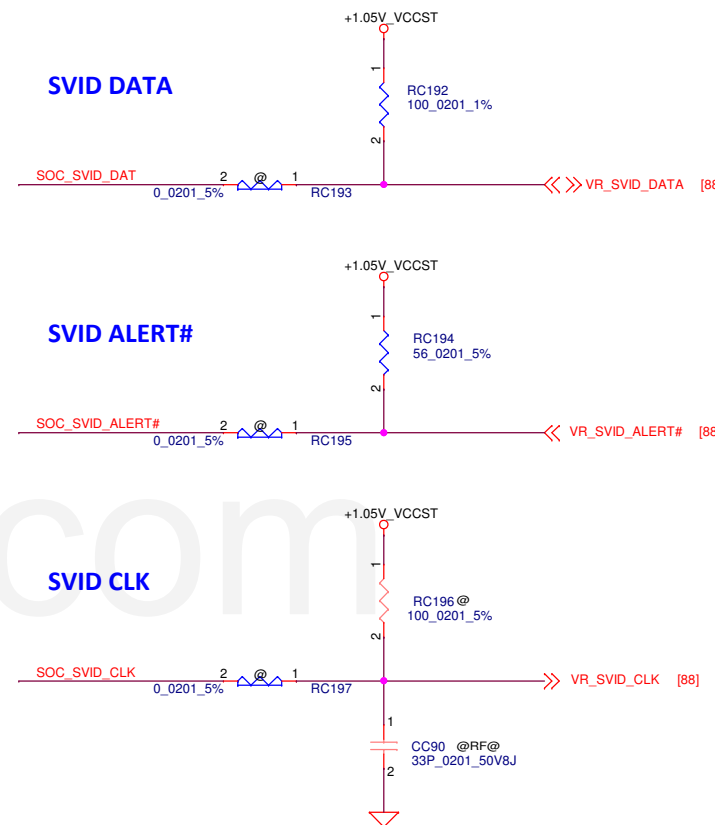
CNV_BRI_CTX_DRX
XTAL SEL
0 = 38.4/19.2MHZ (DEFAULT)
1 = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
WEAK INTERNAL PD 20K



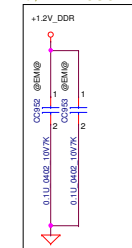
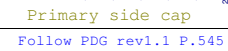
Main Function: CPU(9/13)



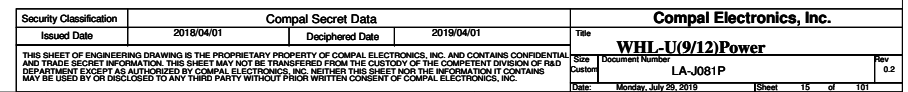
- 1.The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
 - 2.Route the Alert signal between the Clock and the Data signals.
- CAD Note: Place the PU resistors close to CPU

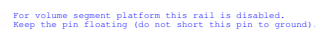


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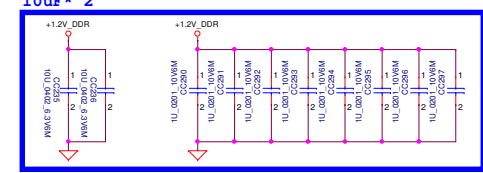


6/14 reserve for EMI request

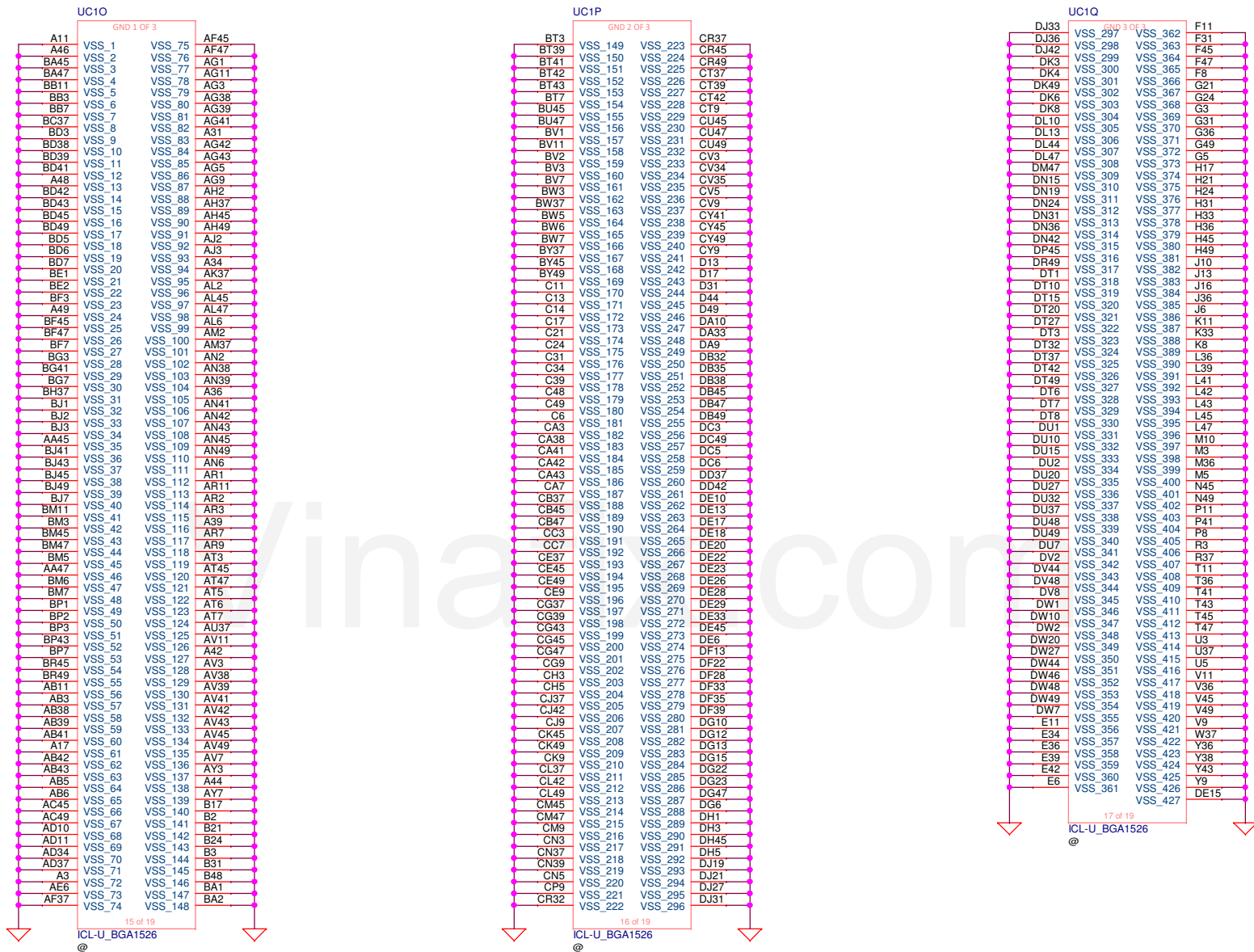




Note: Logic "0" is 0V and Logic "1" is 1.8V based logic, but the VID pins must be 3.3V tolerant as well.

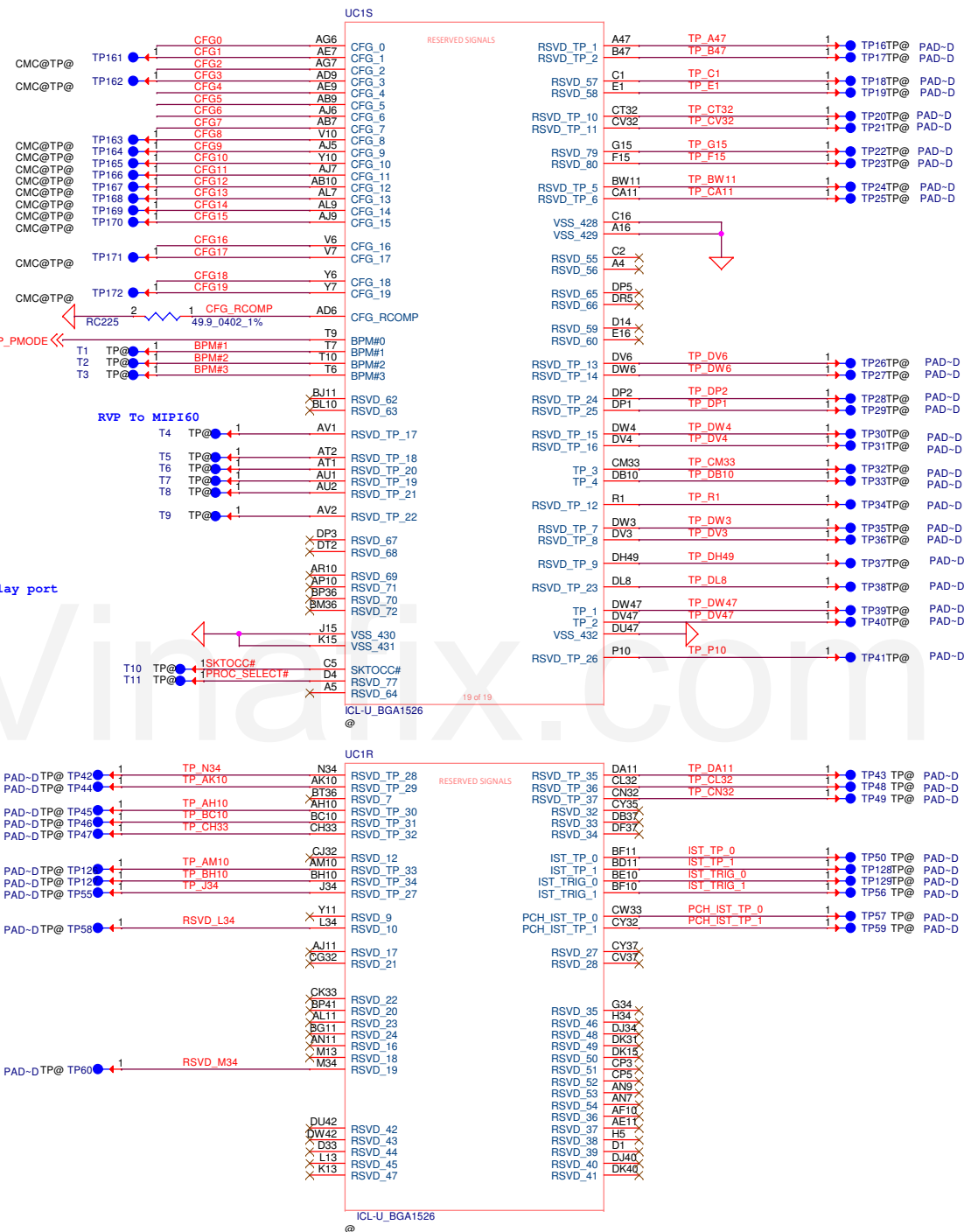
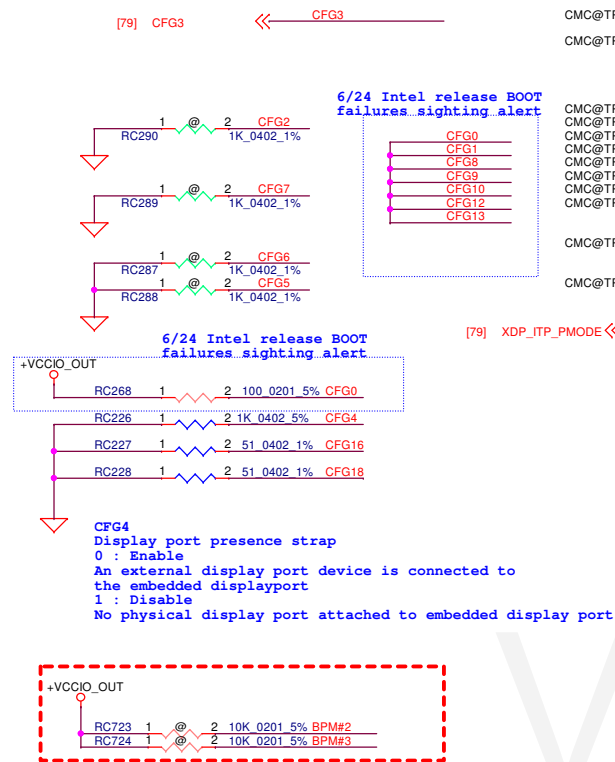


Main Function: CPU(12/13)



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								Size	Document Number			Rev	
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								Date: Monday, Jul 29, 2019			Sheet 17 of 101		

Main Function: CPU(13/13)



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Main Function:

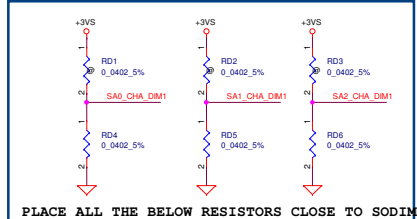
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CHANNEL-M0

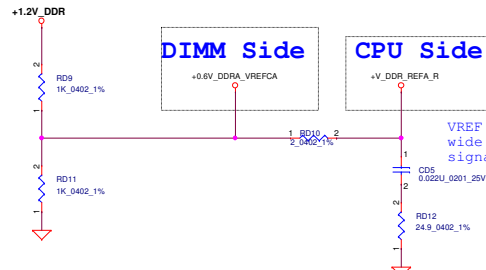
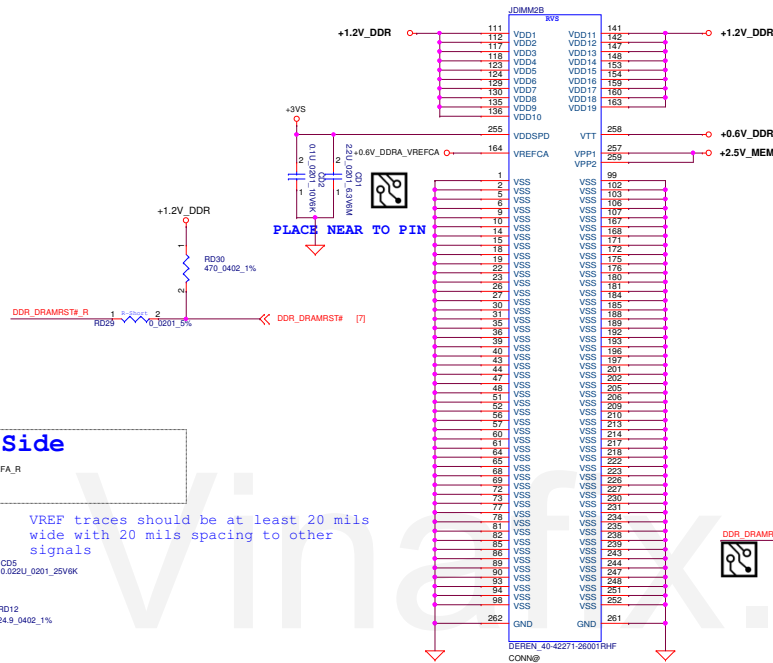
BOT: DIMM1 (JDIMM2 CONN) Non-ECC DIMM



SPD ADDRESS FOR CHANNEL A :
SA0 = 0; SA1 = 0; SA2 = 0.

Non-Interleaved Memory

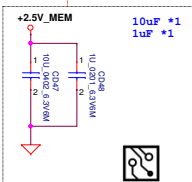
- [7] DDR_M0_DQ0..15
- [7] DDR_M0_DQ16..31
- [7] DDR_M0_DQ32..47
- [7] DDR_M0_DQ48..63



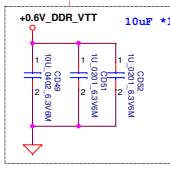
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Decoupling Cap_Channel A

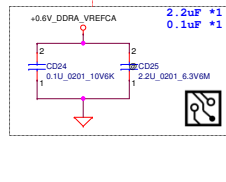
Layout Note:
Place near JDIMM2.257,259



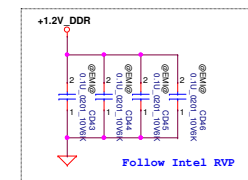
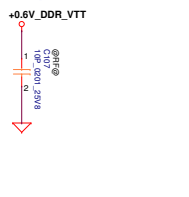
Layout Note:
Place near JDIMM2.258



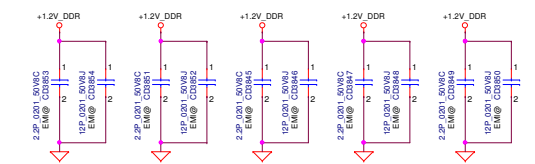
Layout Note:
PLACE THE CAP near JDIMM2.164



C107 place near JDIMM2



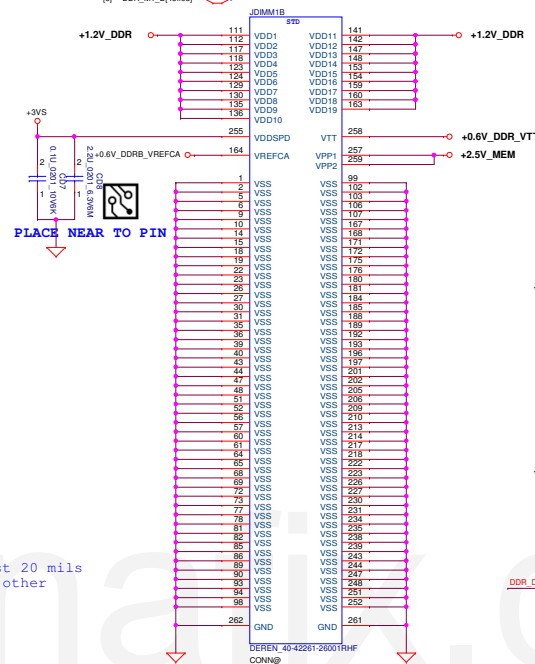
EMC CAPS-PLACE
< 4mm from SO-DIMM VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)



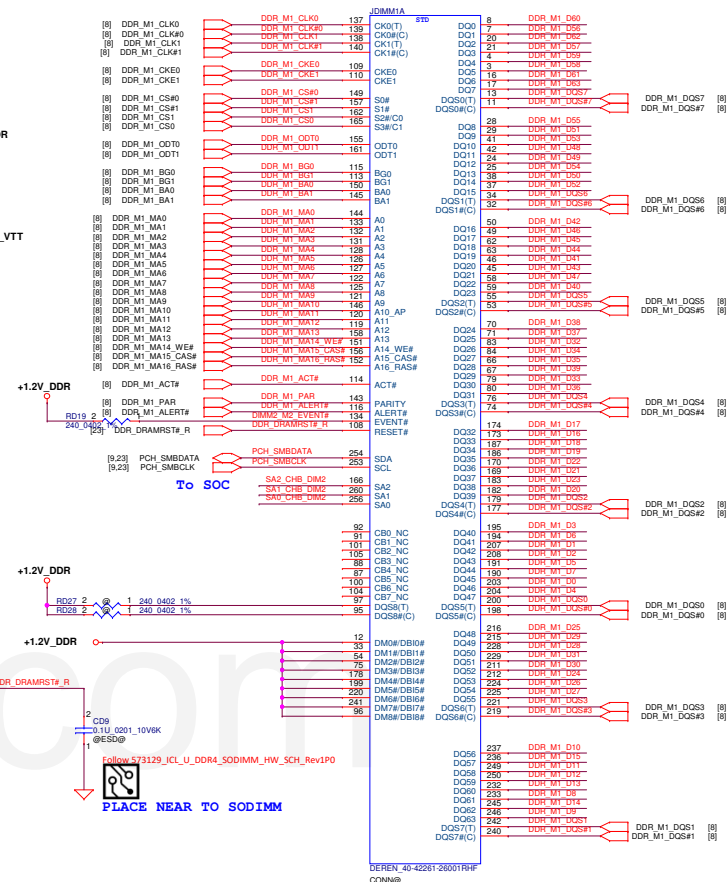
CHANNEL-M1

Non-Interleaved Memory

STD (5.2 mm)

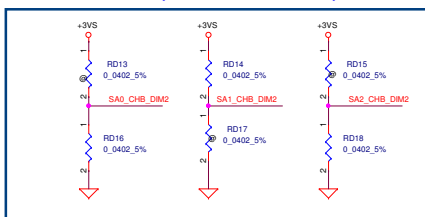


PLACE NEAR TO PIN



PLACE NEAR TO SODIMM

BOT: DIMM2 (JDIMM1 CONN) Non-ECC DIMM



Main Function:

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Main Func = GPU

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Compal Electronics, Inc.

NV(1/5)-PCIE

LA-J081P

Main Func = GPU

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NV(2/5)-IFP_ABCDEF_DAC_XTAL
LA-J081P

Main Func = GPU

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						NV(3/5)-POWER
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Main Func = GPU



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Main Func = GPU

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Main Func = VRAM

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Main Func = VRAM

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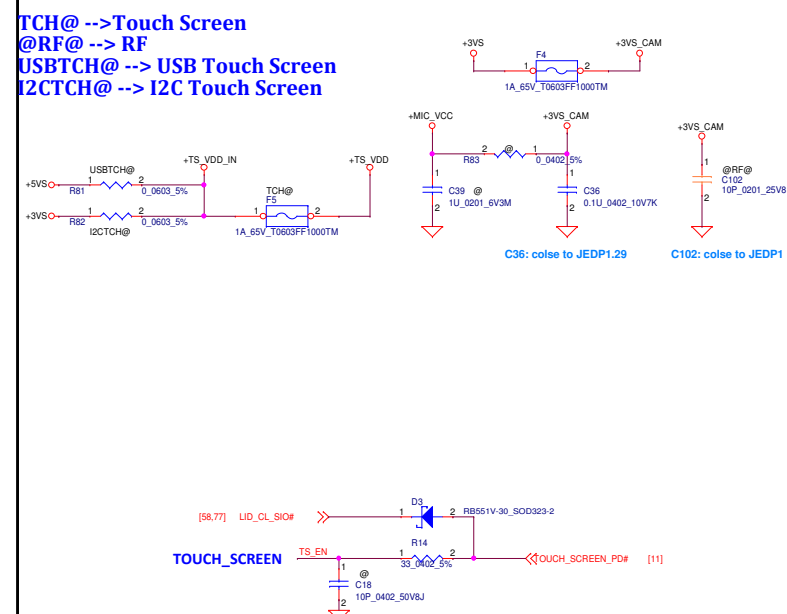
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Main Func = GPU DC

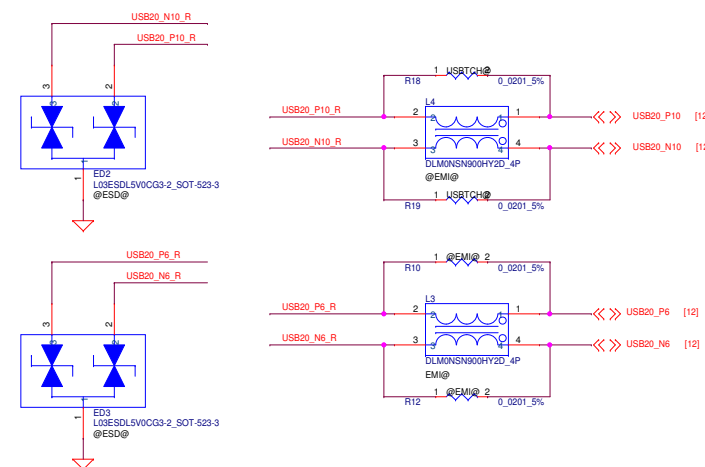
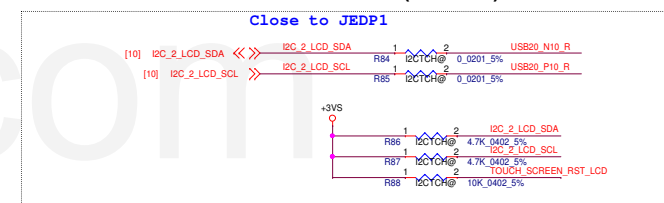
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2
Main Func = CAM&MIC, TS



I2C Touch Screen (Reserved)

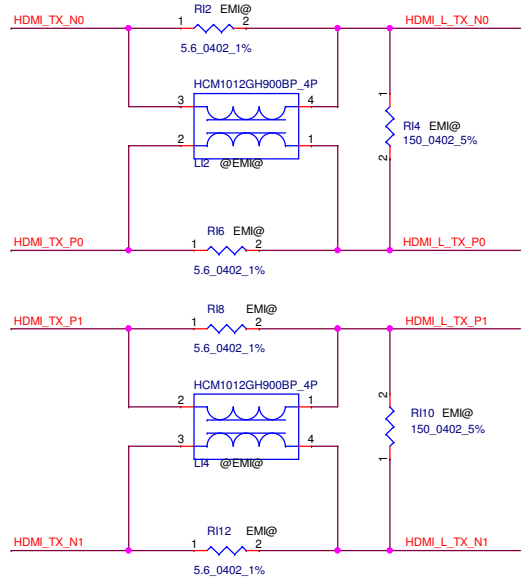
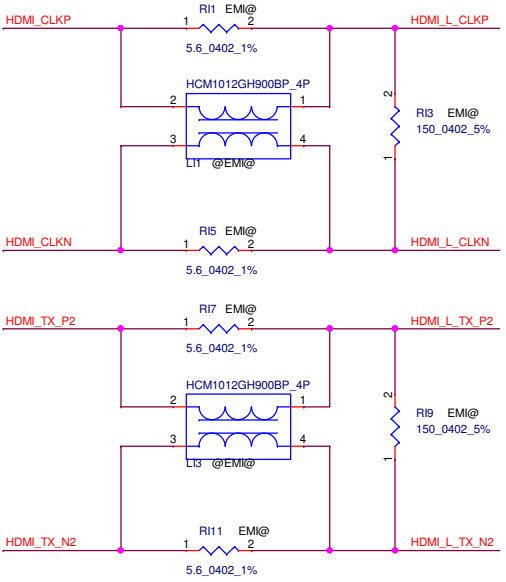
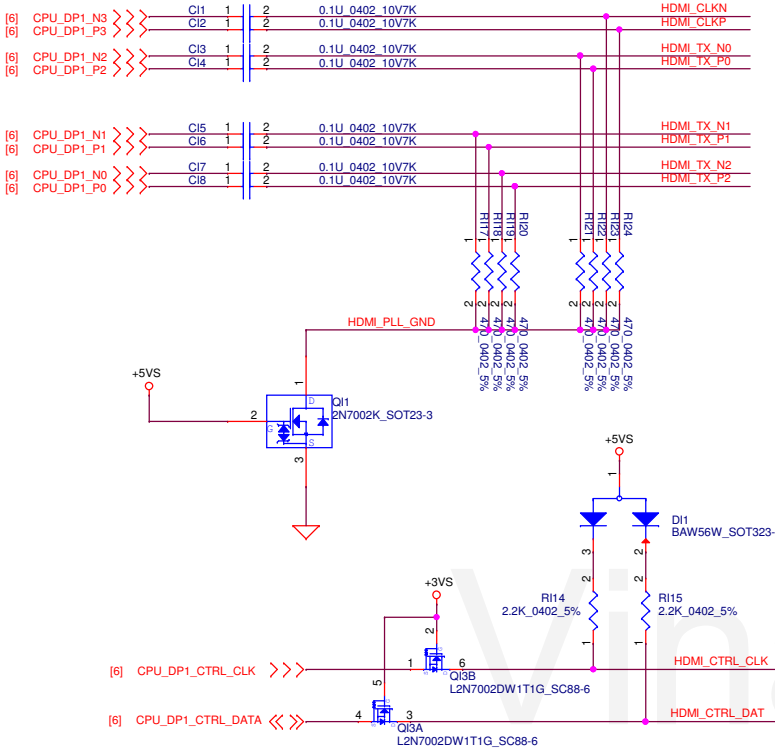


Main Function:

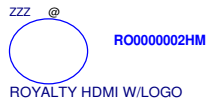
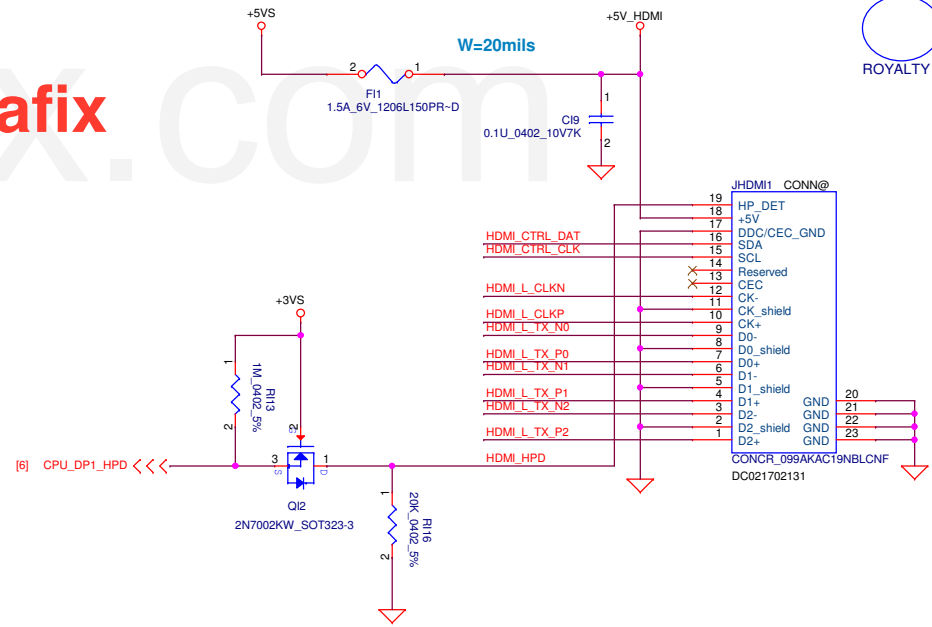
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Main Func = HDMI



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					LA-J081P	0.2
				Date	Monday, July 29, 2019	Sheet 40 of 101

Main Function:

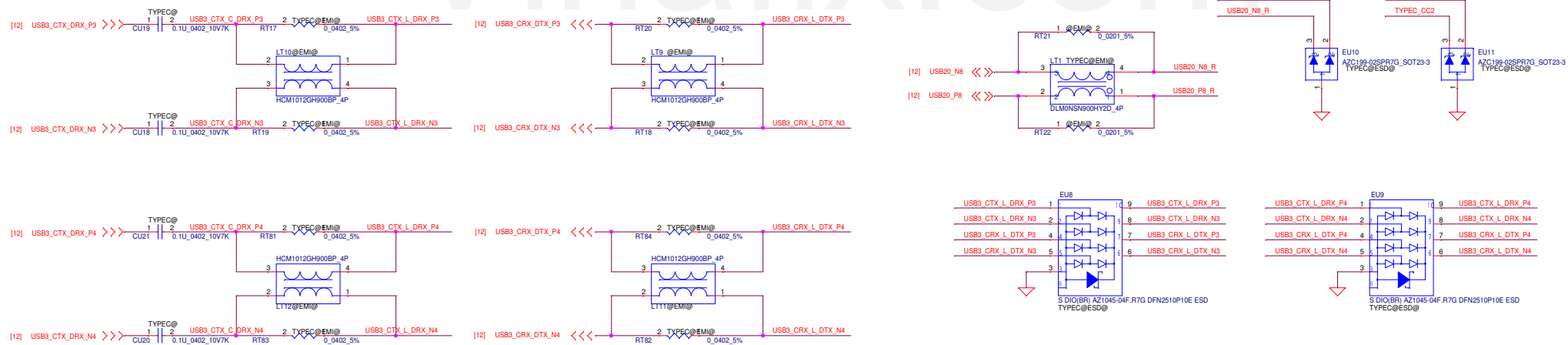
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					LA-J081P	0.2
				Date:	Monday, July 29, 2019	Sheet 48 of 101

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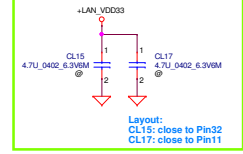
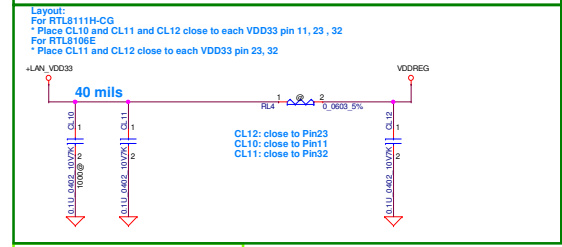
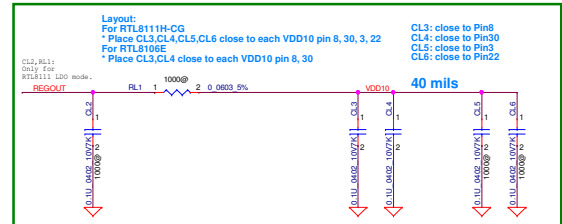
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					LA-J081P	0.2
				Date:	Monday, July 29, 2019	Sheet 49 of 101

Main Function:

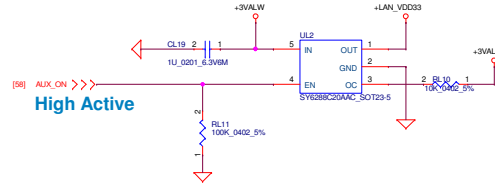
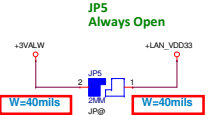
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					LA-J081P	0.2
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Main Func = LAN



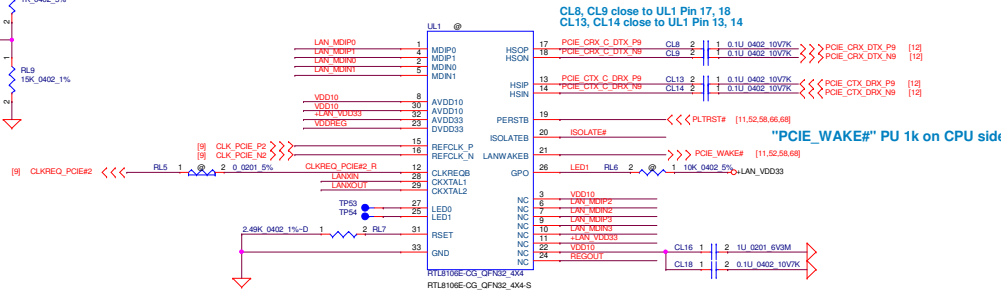
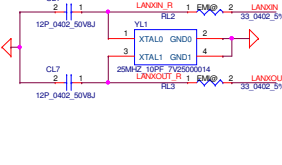
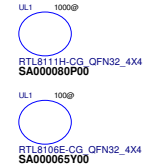
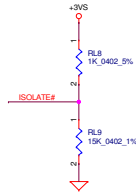
+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



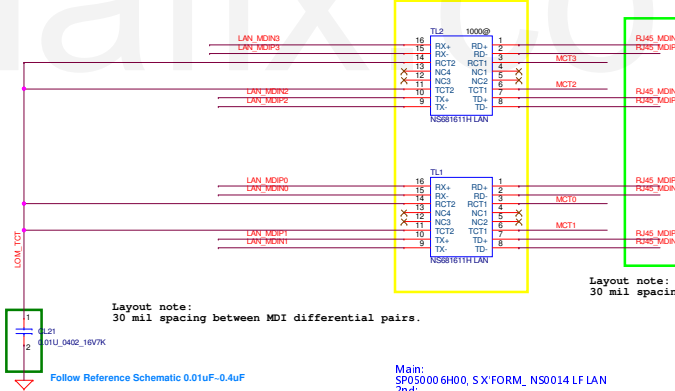
	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

LAN CHIP 10/100/1000

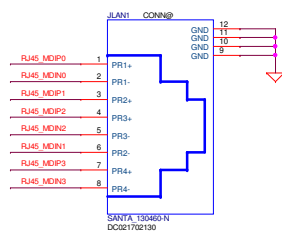
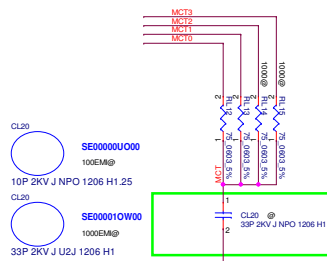
RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M



Main Func = LAN LAN TransFormer 10/100M x2

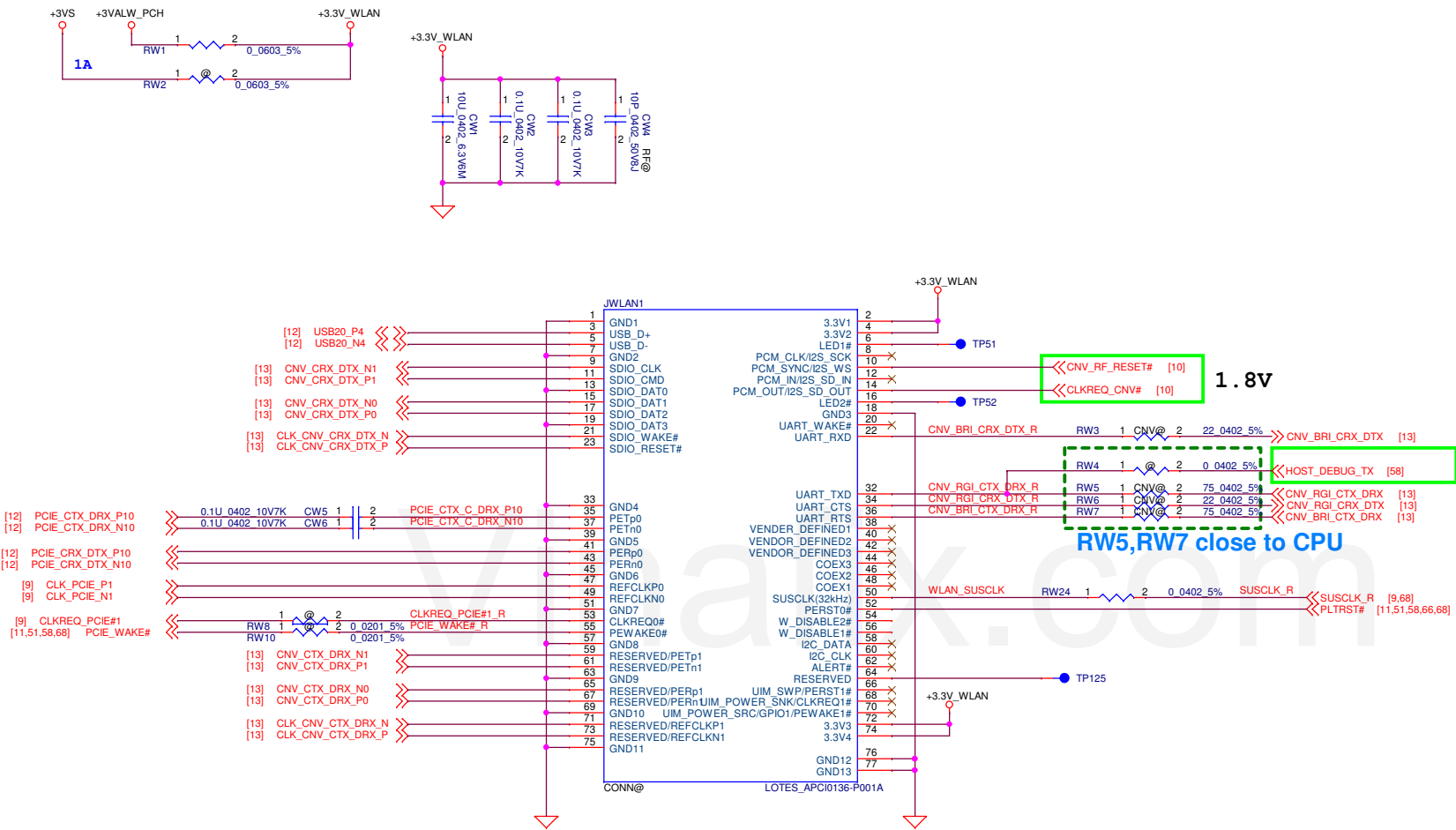


TL1 TOP, TL2 BOT



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Main Func = WLAN E Key CONN



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				Size	Document Number	Rev
					LA-J081P	0.2
				Date:	Monday, July 29, 2019	Sheet 53 of 101

Main Function:

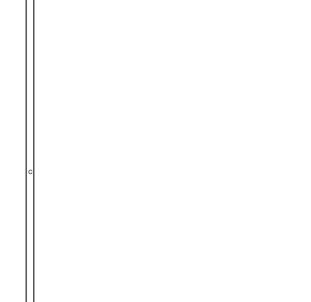
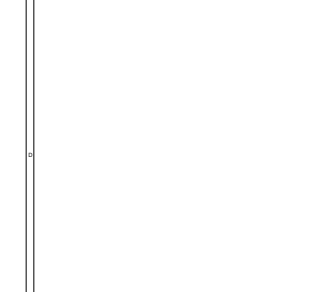
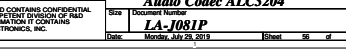
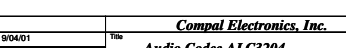
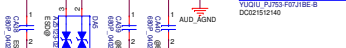
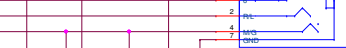
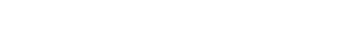
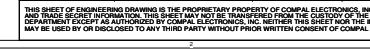
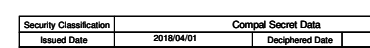
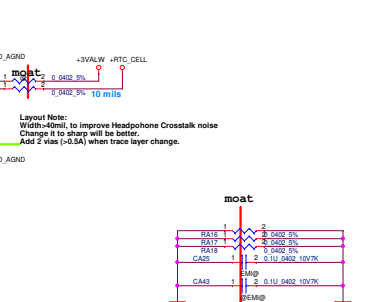
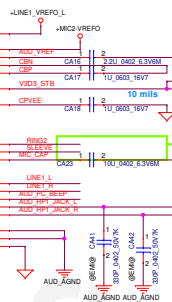
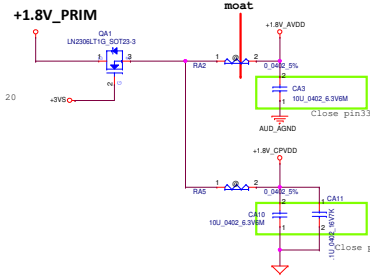
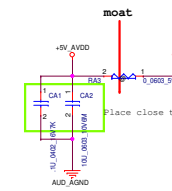
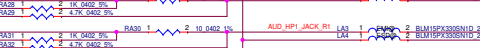
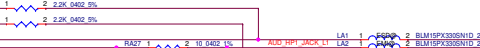
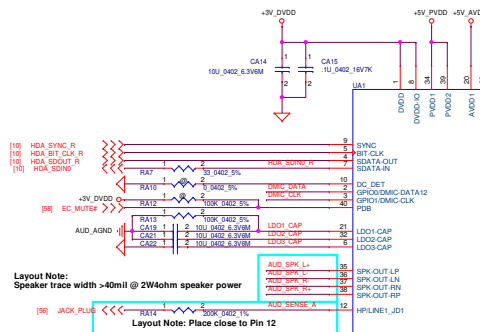
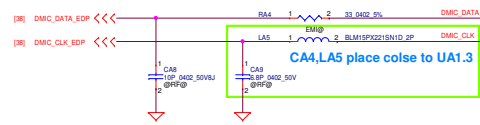
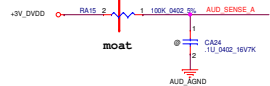
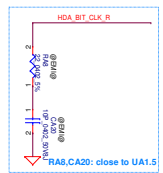
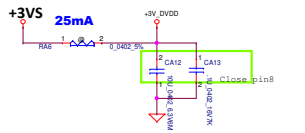
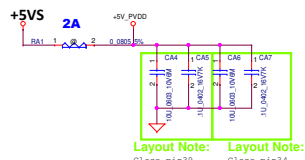
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				Date:	Monday, July 29, 2019	Sheet 54 of 101

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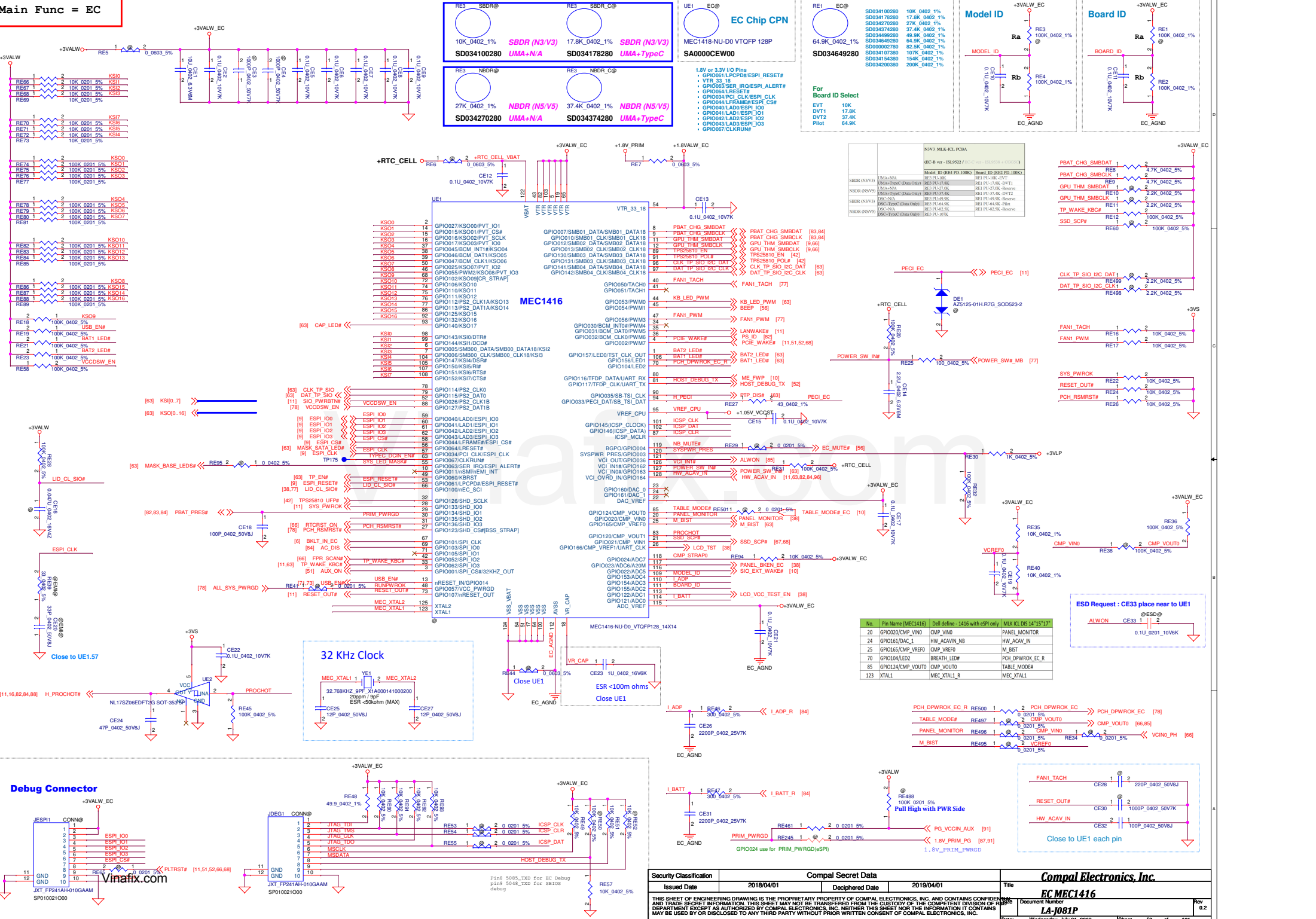
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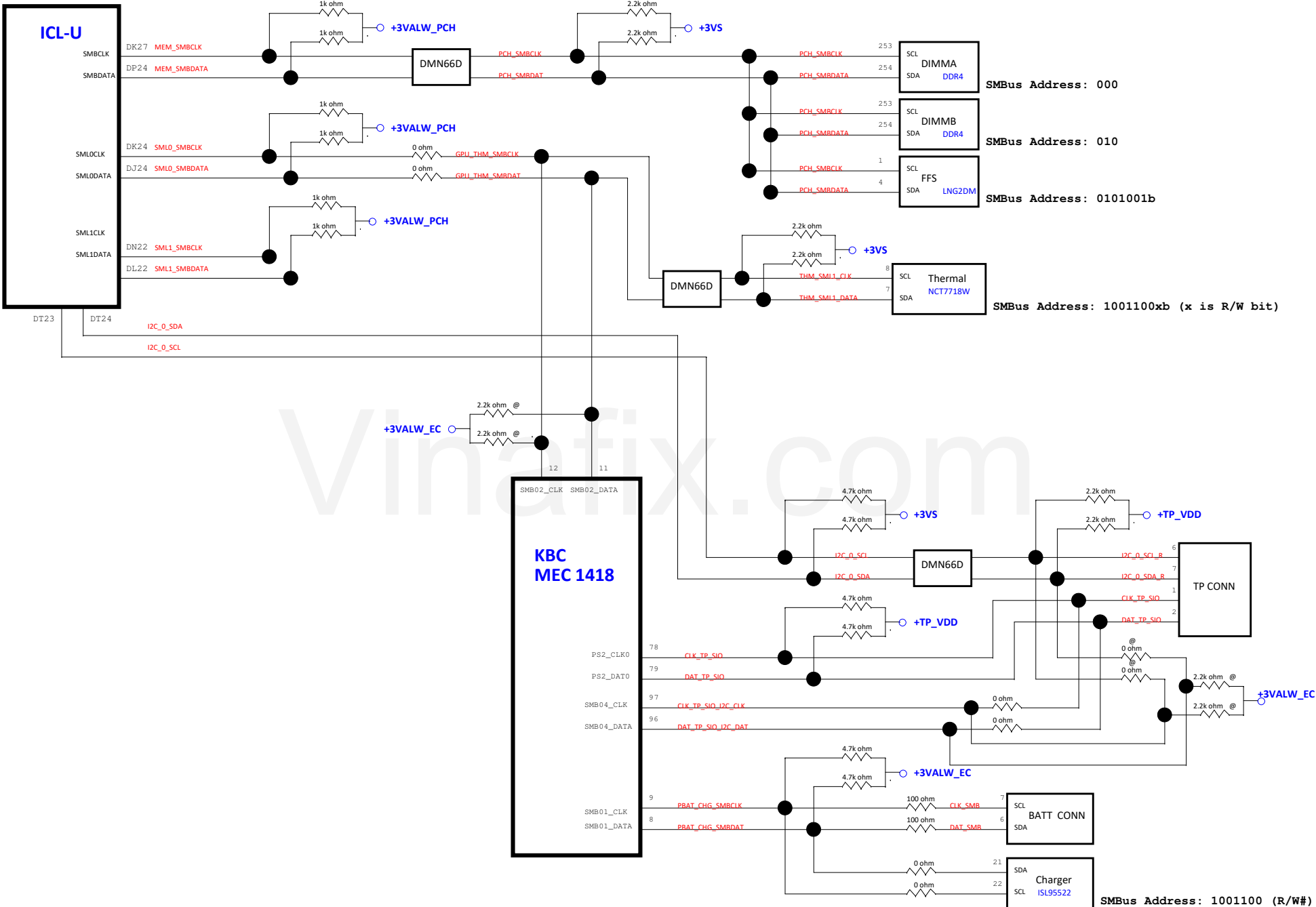
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					LA-J081P	0.2
				Date:	Monday, July 29, 2019	Sheet 60 of 101

Main Function:SMB/I2C Block Diagrams

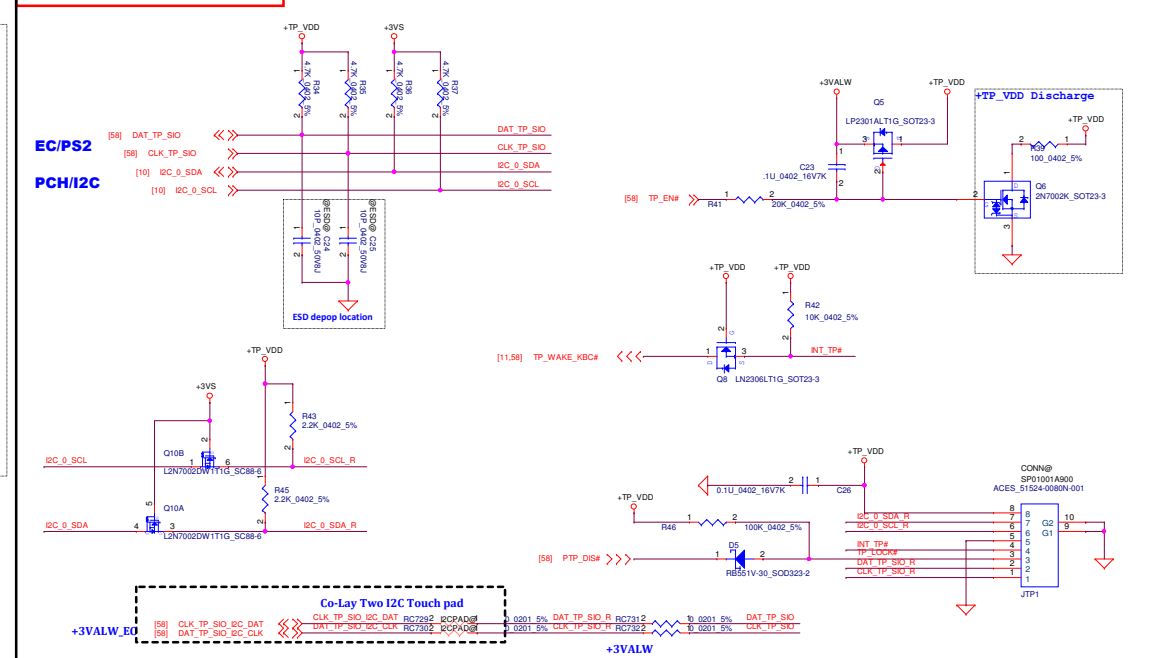
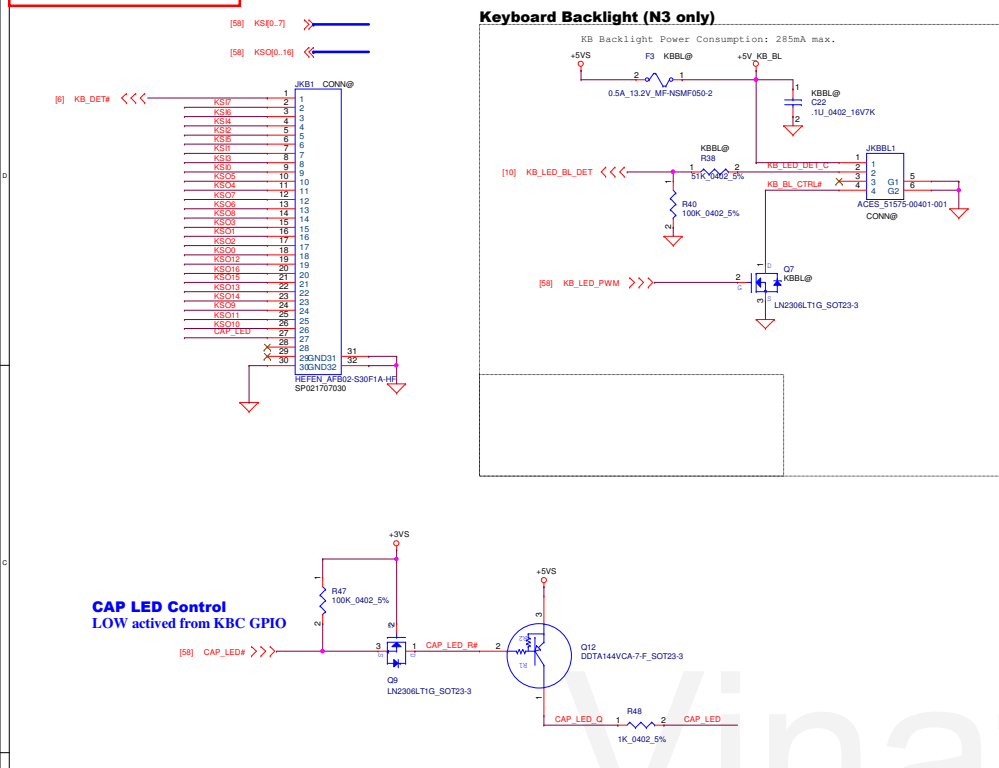


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					LA-J081P	0.2
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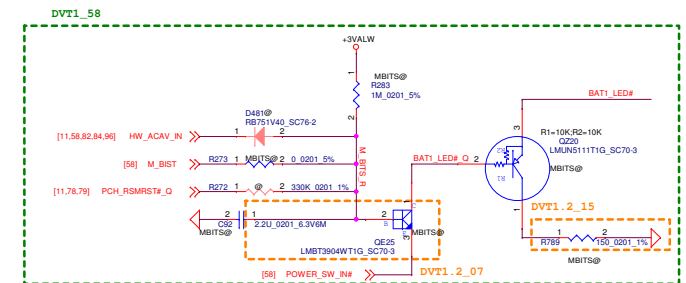
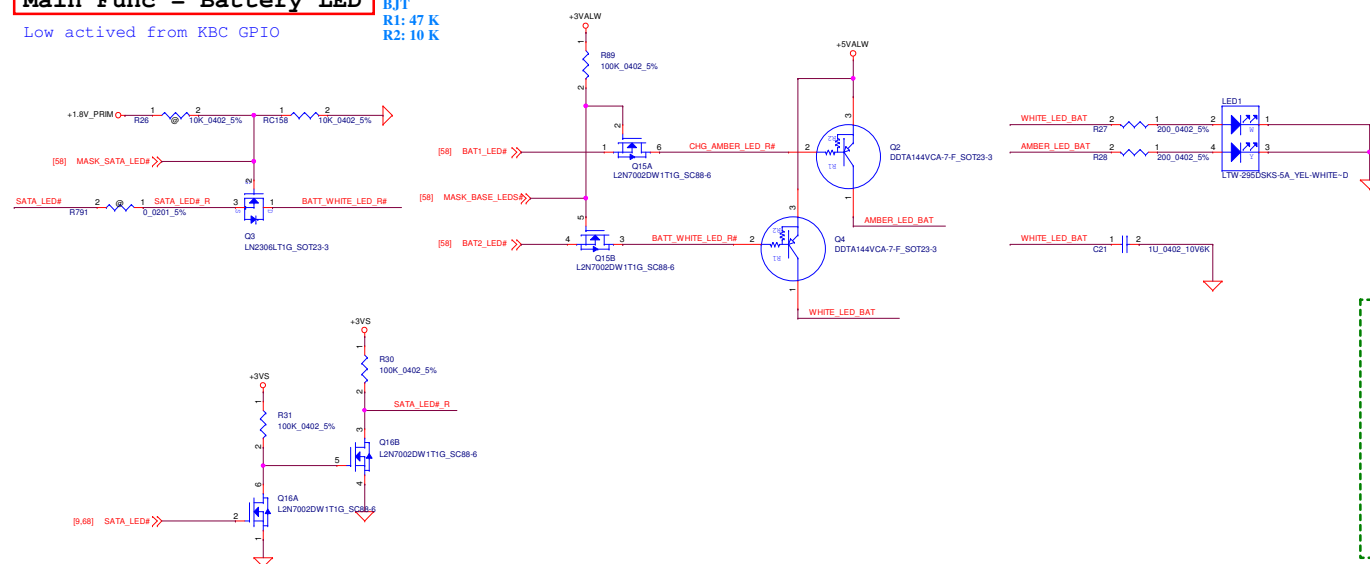
3
Main Func = TPA



Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



Main Function:

Reserve

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				Size	Document Number	Rev
					LA-J081P	0.2
				Date:	Monday, July 29, 2019	Sheet 64 of 101

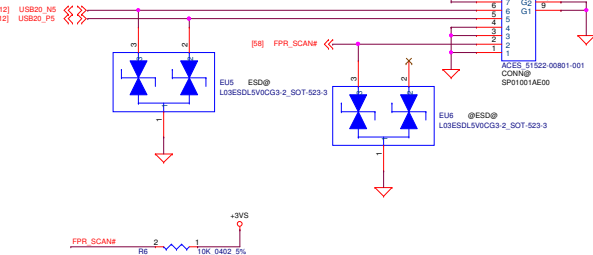
Main Function:

Reserve

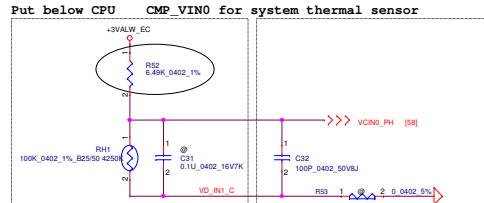
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					LA-J081P	0.2
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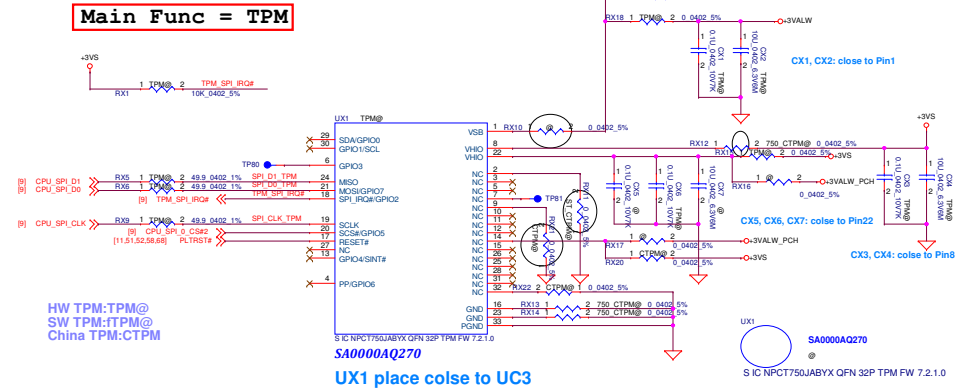
Main Func = FPR



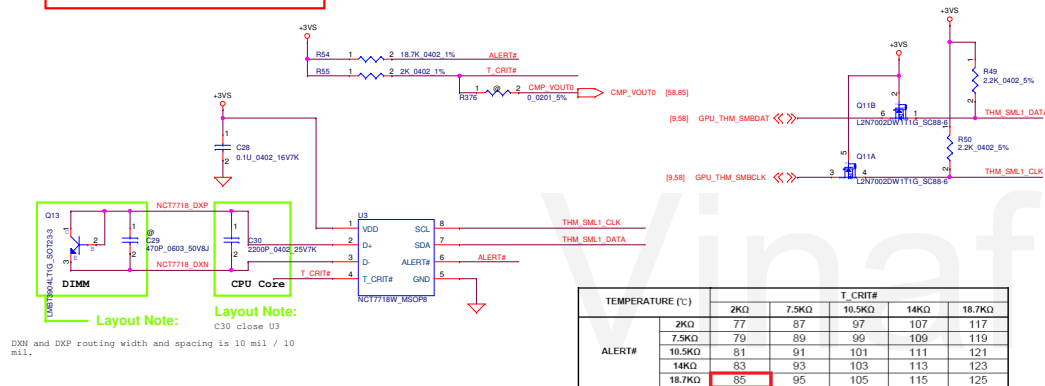
Main Func = OTP



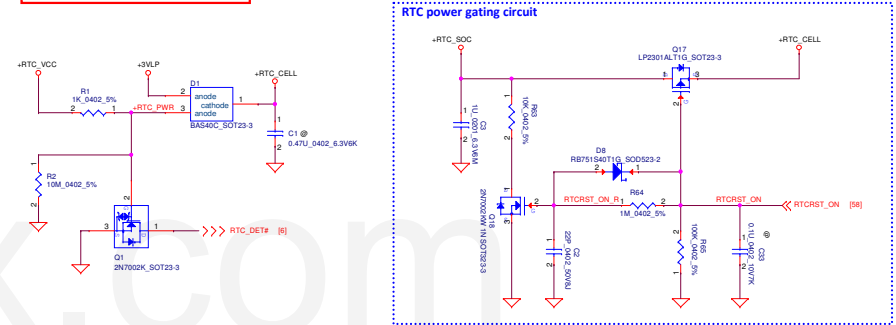
Main Func = TPM



Main Func = Thermal



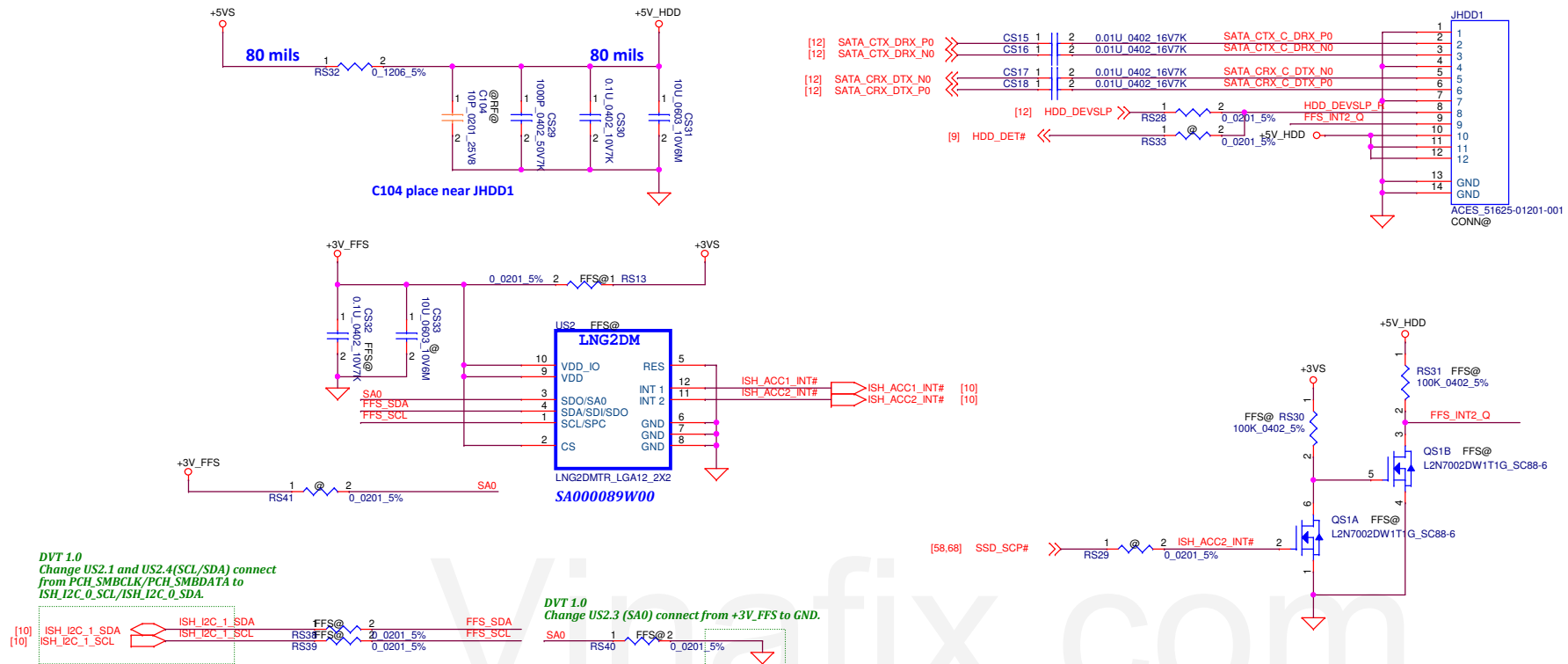
Main Func = RTC



TEMPERATURE (°C)		T CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

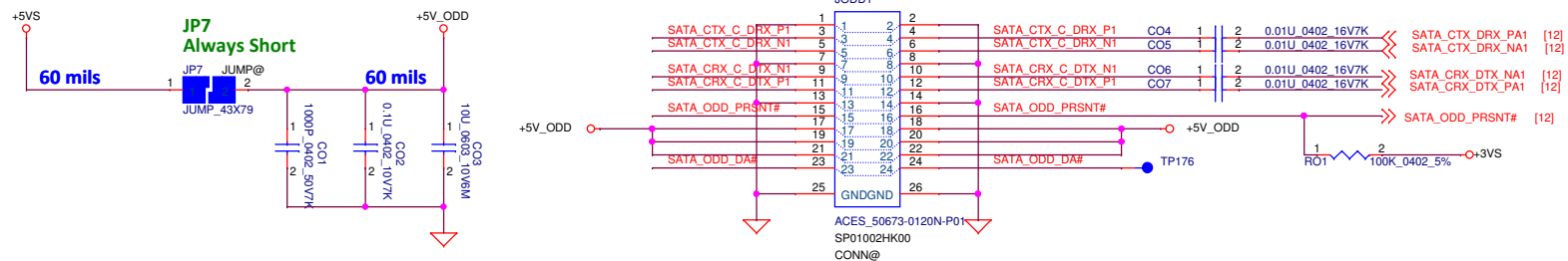
Security Classification	Compul Secret Data		Title		Compul Electronics, Inc.	
Issued Date	2018/04/01	Deciphered Date	2018/04/01	TPM/RTX/Screw hole		
<p>THIS SET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPUL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED OUTSIDE OF THE COMPETITIVE DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPUL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPUL ELECTRONICS, INC.</p>				Size	Docuement Number	Rev
					LA-90819	0.2
Date				Monday, July 29, 2019	Sheet	68 of 101

Main Func = HDD&FFS



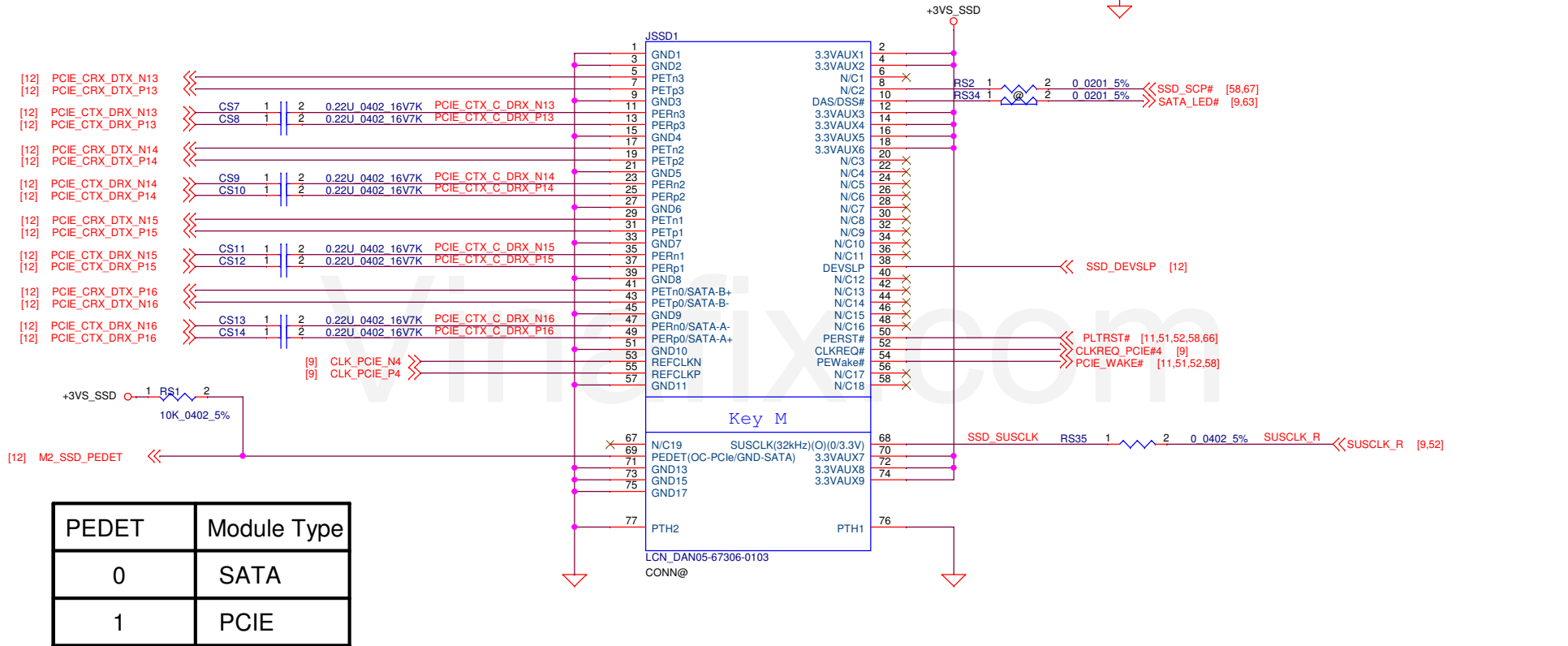
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	8
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	9

Main Func = ODD



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSENT	P1	8
5V	P2	9
5V	P3	10
5V	P3	11
Attention	P4	12
GND	P5	
GND	P6	

NGFF Key M



Main Func = eMMC

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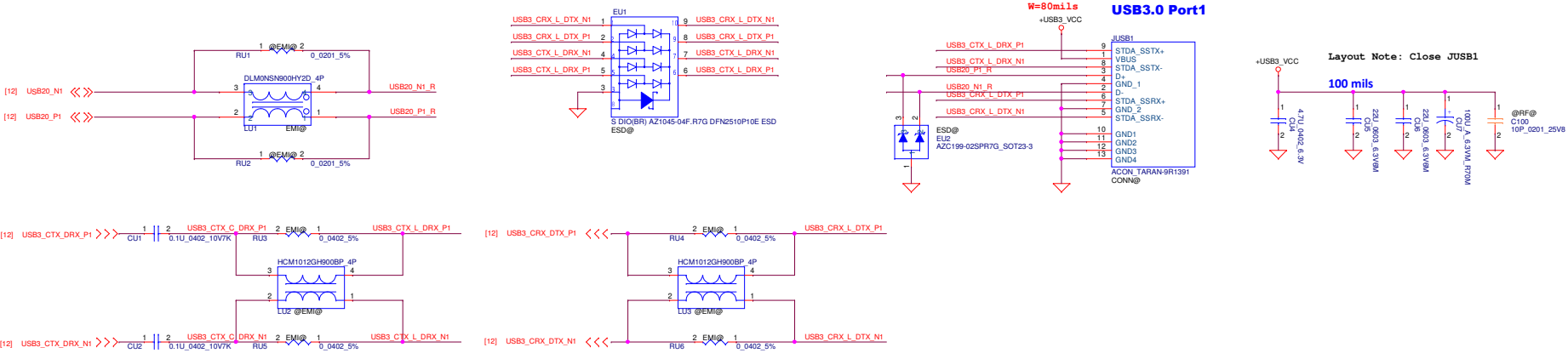
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2018/04/01		2019/04/01		Document Number	
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		Monday, July 29, 2019		0.2	
		Sheet		of	
		69		101	

Main Function:

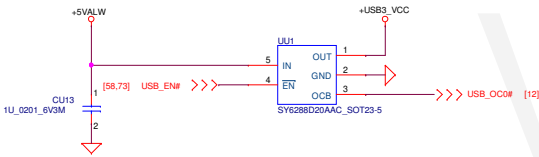
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					LA-J081P	0.2
				Date:	Monday, July 29, 2019	Sheet 70 of 101

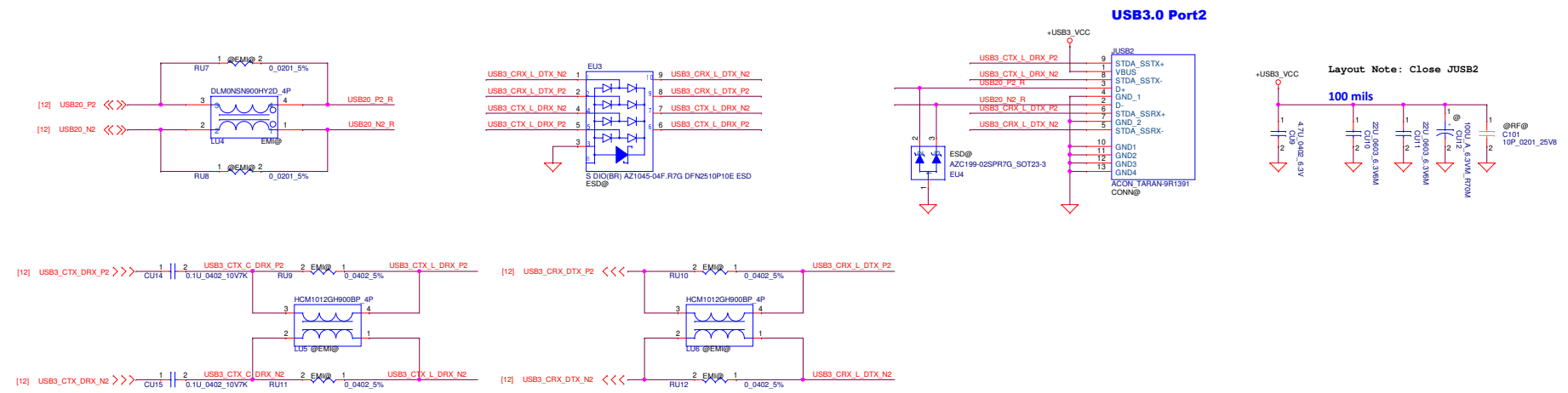
Main Func = USB3.0 Port1



Maximum Output Current 2A



Main Func = USB3.0 Port2

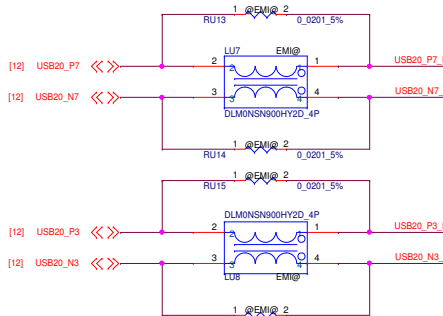
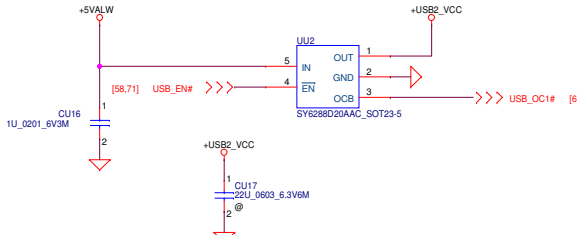


Main Function:

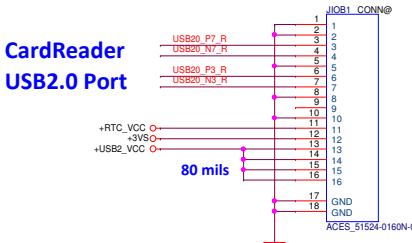
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Main Func = USB2.0 Port3 + Card Reader on IO/B



USB2.0/Card Reader connector



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				LA-J081P Date: Monday, July 29, 2019	Rev 0.2
				ISheet	73 of 101

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				Size	Document Number	Rev
					LA-J081P	0.2
				Date:	Monday, July 29, 2019	Sheet 75 of 101

Main Function:

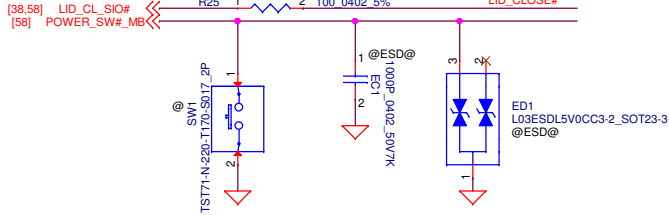
Reserve

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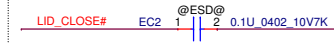
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title		
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				Size	Document Number	Rev
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				Date:	Monday, July 29, 2019	Sheet 76 of 101

Main Func = Power BTN

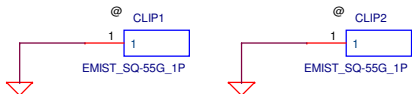
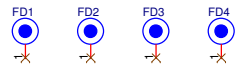
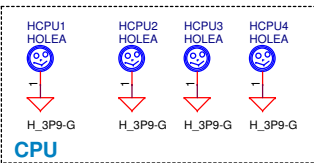
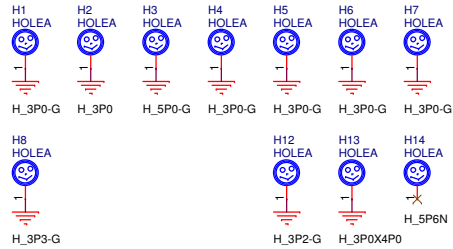
Low activated from KBC GPIO



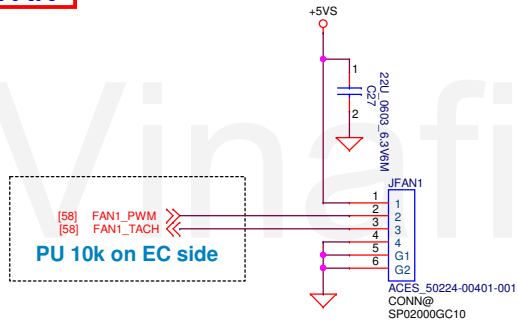
For EMI Reserved



Screw hole/FD

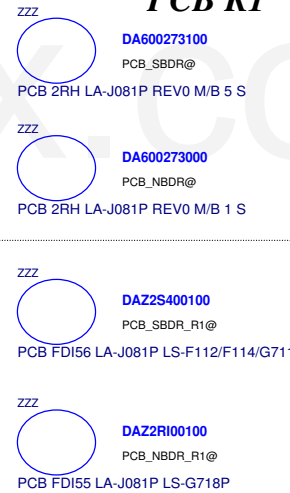


FAN

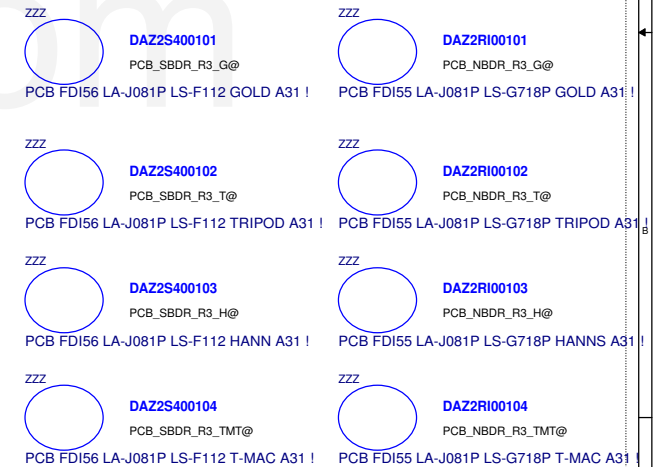


PCB PN

PCB R1



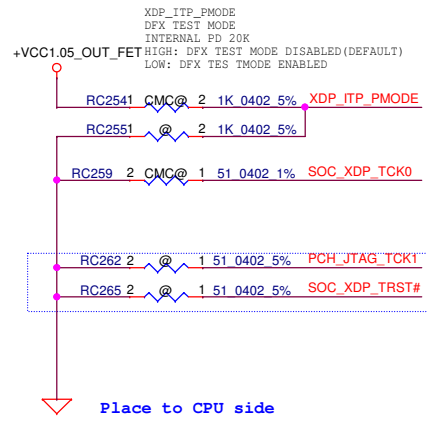
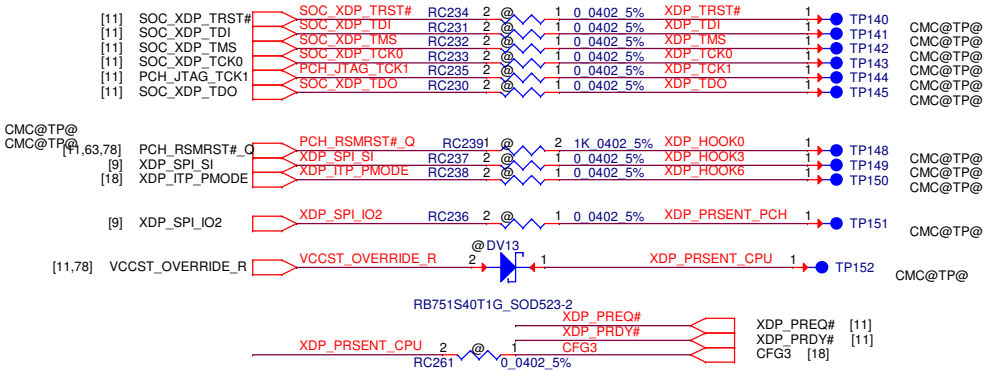
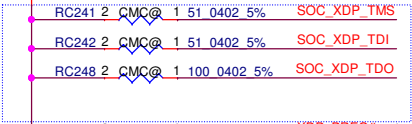
PCB R3



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Main Func = Power Monitor

+1.05V_VCCSTG



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				Rev	0.2
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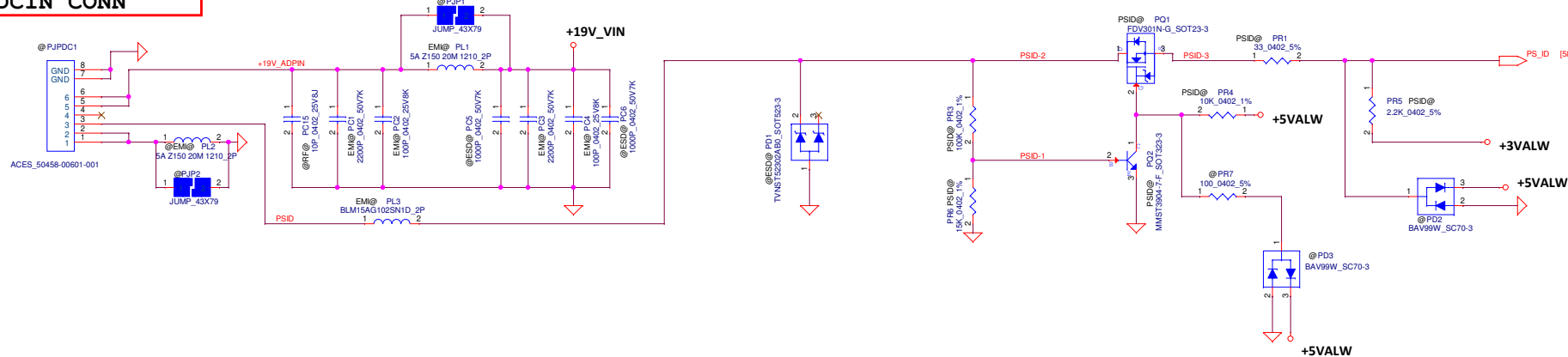
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				Size	Document Number	Rev
				B	LA-J081P	0.2
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Reserve

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				Size	Document Number
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Main Func = DCIN CONN



Battery Bot Side

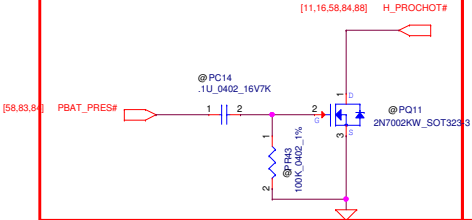
PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220

ACES_50458-01001-P01_10P-T

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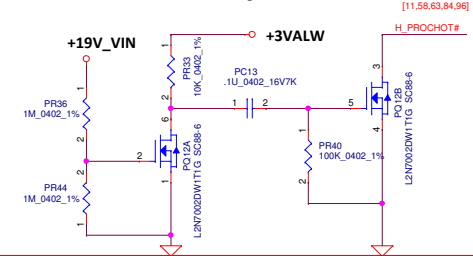
Adapter protection:

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

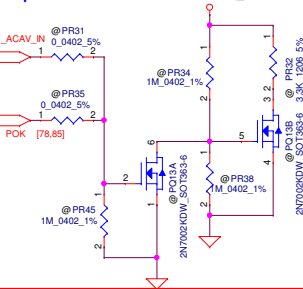


Battery protection:

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW PROCHOT# is issued by EC



Erp lot6 Circuit

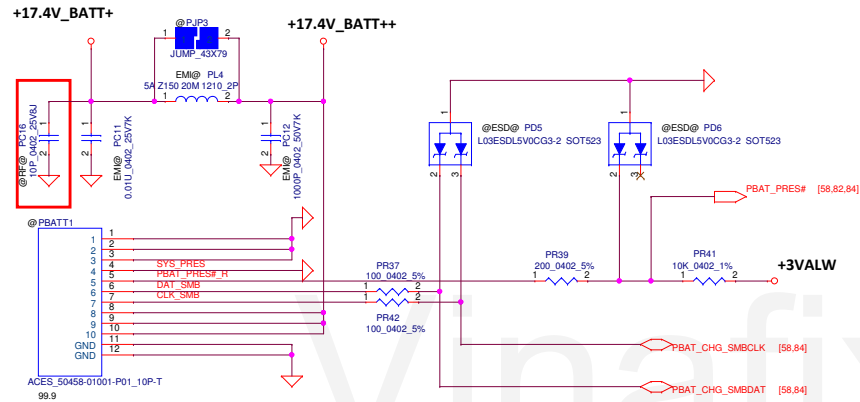


Main Func = BATT CONN

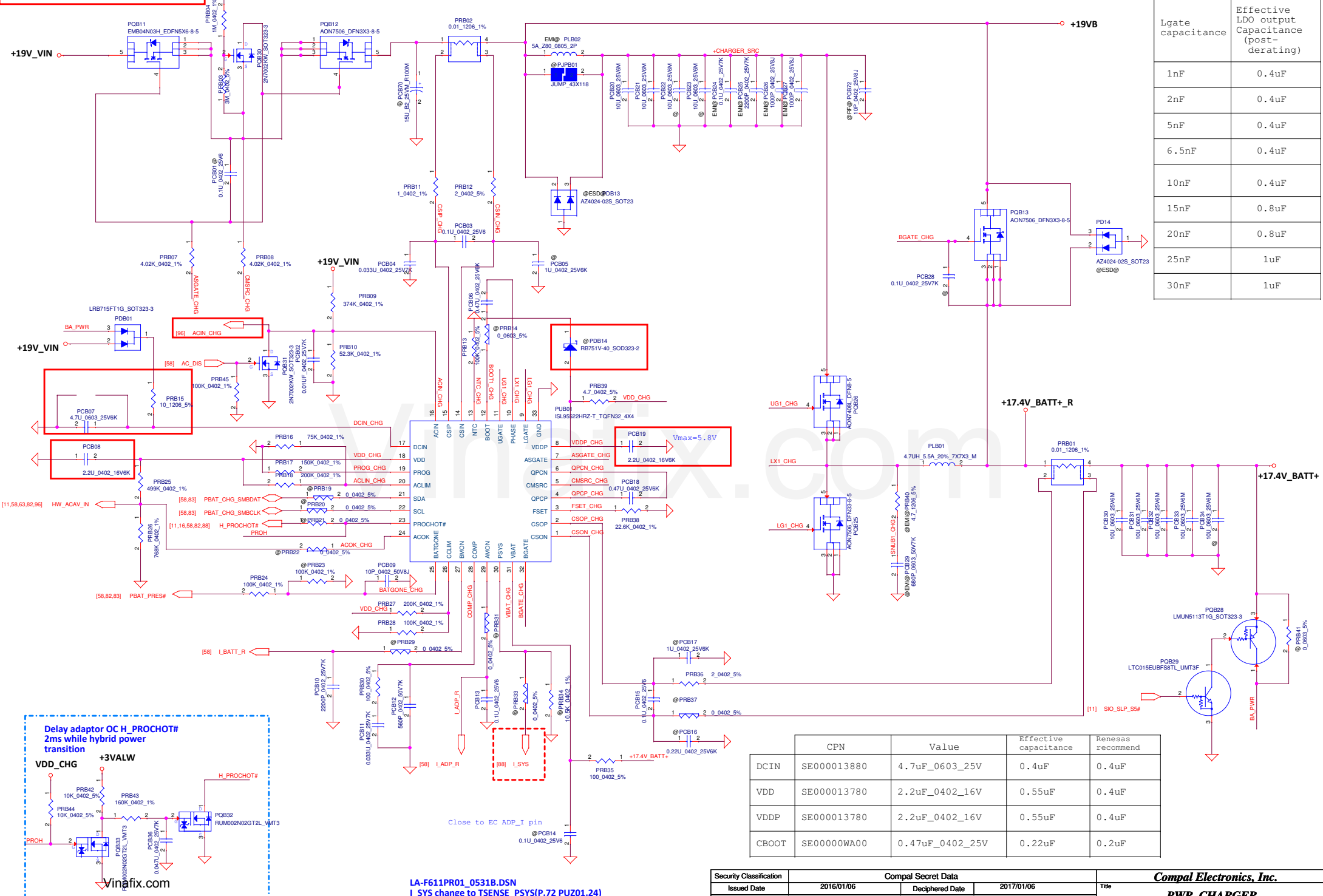
Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220

ACES_50458-01001-P01_10P-T



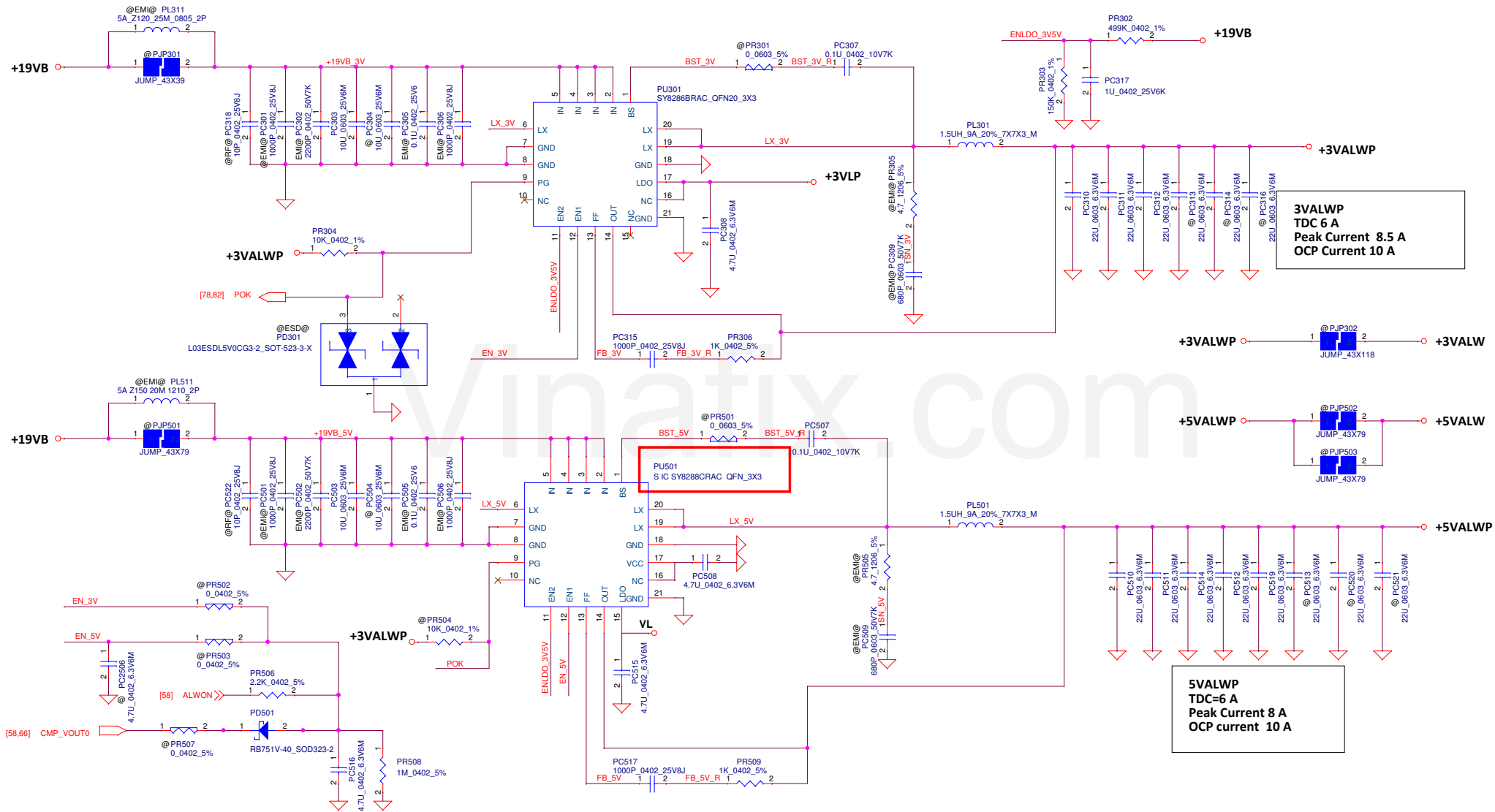
Main Func = CHARGER



Lgate capacitance	Effective LDO output Capacitance (post-derating)
1nF	0.4uF
2nF	0.4uF
5nF	0.4uF
6.5nF	0.4uF
10nF	0.4uF
15nF	0.8uF
20nF	0.8uF
25nF	1uF
30nF	1uF

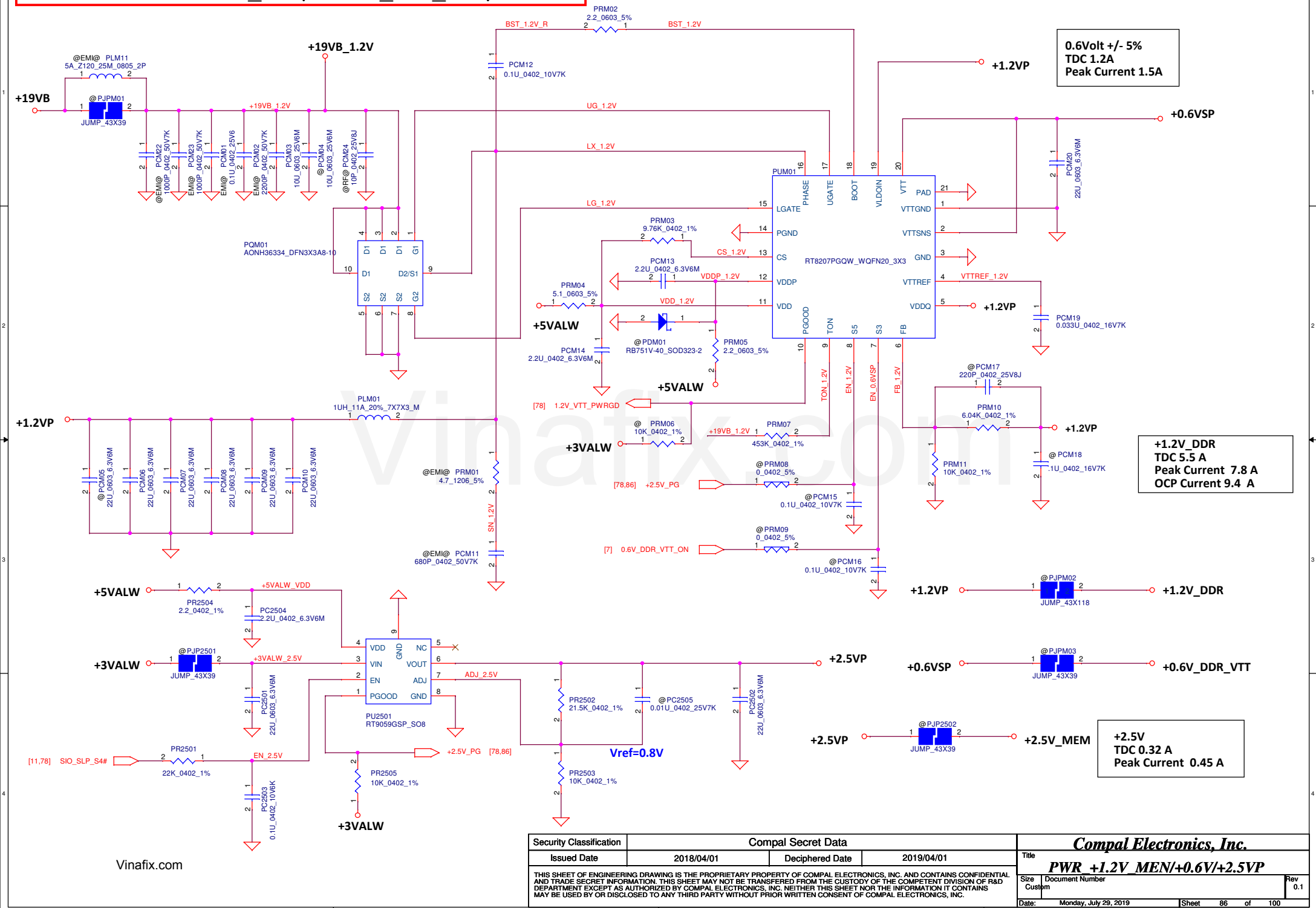
	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF	0.2uF

Main Func = 3.3VALWP/5VALWP

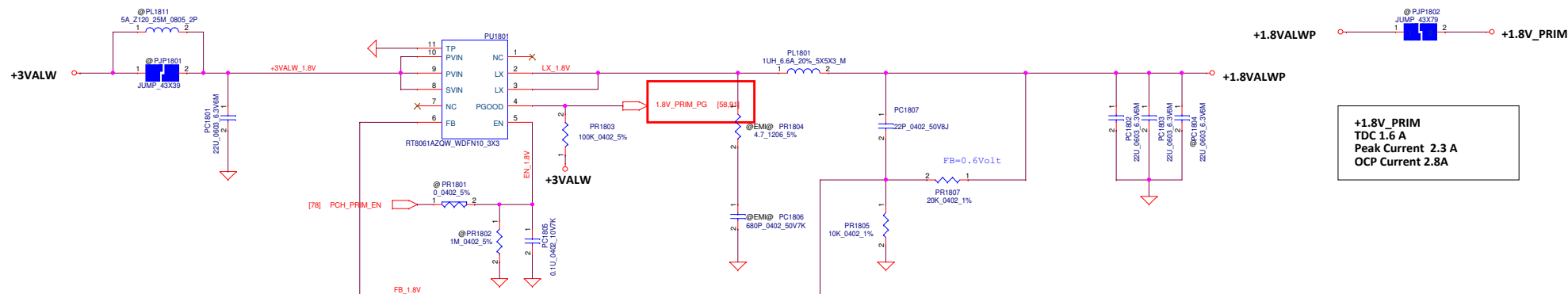


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Main Func = +1.2V_DDR/+0.6V_DDR_VTT/ +2.5VP



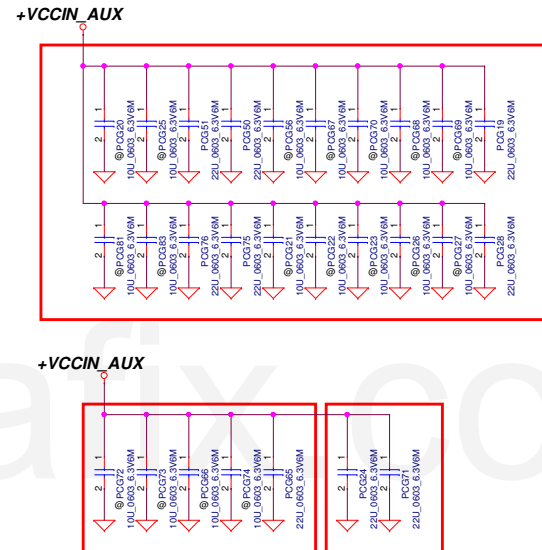
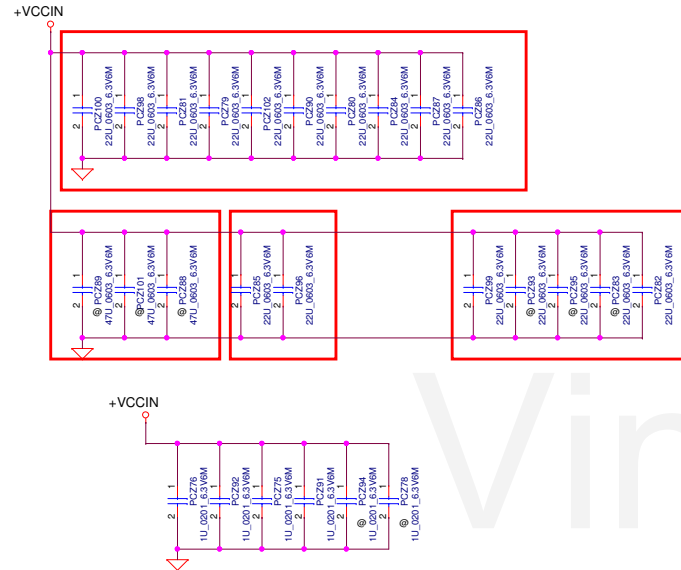
Main Func = +1.8VALWP / +1.05VALWP



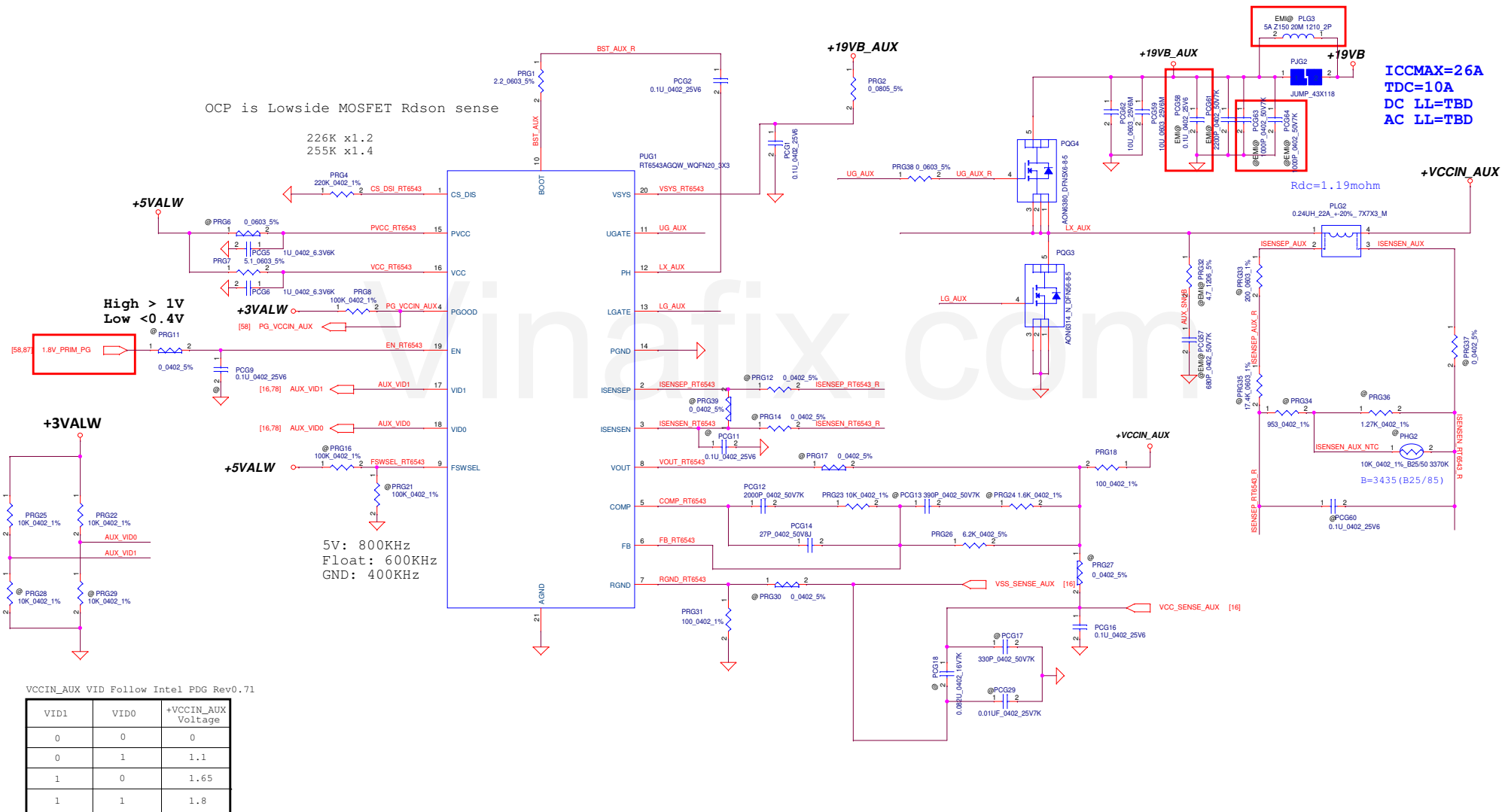
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OCP=91
ICCMAX=70A
TDC=39A

Vinafix.com



Main Func = VCCIN_AUX



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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P83	BATT CONN	20190423	COMPAL	RF request for RF test	Reserve PC16	0.2 (X01)
2	P84	PWR CHARGER	20190423	COMPAL	"Based on Loki G issue, change to follow Renesas recommendation"	1. PCB07 change to 0603 2. Remove PCB71 3. PRB15 change to 1206	0.2 (X01)
3	P96	NO SMOKE	20190423	COMPAL	customer request	Add page 96: reserve NO SMOKE schematic	0.2 (X01)
4	P88	PWR VCCIN	20190507	COMPAL	Change RC value for Intel EA test	"Change RC value for Intel test: PCZ77=330UF PCZ79/80/81/82/84/85/86/87/90/96/98/99/100/102=22uF VCCAUX Output caps 1+9 PCG46=330UF PCG19/24/28/50/51/65/71/75/76=22uF PRZ14/25=2.21Kohm PRZ13/24=2.05kohm PRZ17/26=3.01Kohm PRZ48=37.4Kohm PRZ66=200ohm PRZ49=12.1Kohm PRZ53=14.7kohm PCZ10=82pF PCZ11=220pF "	0.2 (X01)

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0.1

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DVT1 EE change list

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout
Based on 05/15								
1	2018/5/17	8		Add RC207, CPU_SPL_0_CS#1	For 2nd ROM	Y	N	Y
2	2018/5/17	66		Del JP7, short +5VS and +5VS_ODD	Optimal B+ routing	Y	N	Y
3	2018/5/17	14		CC52,CC48,CC51,C5 change to 0402	meet purchase requirement	Y	Y	Y
4	2018/5/17	29		CV73~CV78, CV100~CV109 change to 0402	meet purchase requirement	Y	Y	Y
5	2018/5/17	71		del CU3,CU8 CU4,CU9 1U change to 4,7U	meet purchase requirement	Y	Y	Y
6	2018/5/20			Del CS6,CU3,CU8; CU13,CT16,C8,C35,C39 change to 0201,CT1 change to 0603	MLCC downsize	Y	Y	Y
7	2018/5/25			Del C34,R68,R69,R70,R71; U2 change Footprint	For 17" Touch	Y	N	Y
8	2018/6/4	38		Connect UC1,CC30 to R72, Add RC208,RC209	For 17" Touch	Y	N	Y
9	2018/6/4			C27,CT14,CU10,CU11,CU5,CU6,CU17 change to 0603	MLCC downsize	Y	Y	Y
10	2018/6/4	31		CV161,CV162,CV163,CV164,CV165,CV166,CV167,CV168,CV169,CV170,CV182,CV183,CV184,CV185,CV186,CV187,CV188,CV189,CV190,CV191,CL16 change to 0201	MLCC downsize	Y	Y	Y
11	2018/6/13	56		CA16 change to 0402	MLCC downsize	Y	Y	Y
12	2018/7/4	65		add Rx10~14	co-lay ST TPM	Y	N	Y
13	2018/7/4			add CC75(pop),CZ41,CC76,CC77,CC78,CC79	For ESD requirement	Y	Y	Y
14	2018/7/6	65		add Rx15~RX19	co-lay China TPM	Y	N	Y

DVT2 EE change list

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout
Based on 07/16								
1	2018/8/14	66	RX20,RX21,RX22	reserve 0 ohm 0402	reserve for china TPM	Y	N	Y
2	2018/8/15	38	R96	reserve 0 ohm 0201	disconnect B+	Y	N	Y
3			EU1,EU3,EU8,EU9	SC300002C00=>SC300001Y00	ESD require	Y	Y	N
4		71	RE1	SD034178280=>SD034270280 17.8K change to 27K	EC board ID	Y	Y	N
5			CC54,CC57		fixed 1.05 OV(P)(BITS382716)	Y	Y	N
6			U22	SA00007XR00=>SA00008R600(Vccio load switch)	fixed 1.05 OV(P)(BITS382716)	Y	Y	N
7				Remove Typec configuration	Dell PCR	N	Y	N
8			CC64,CC52,CC59,CC17,CC15,CC18,CC19	0402 1u =>0201 1u	MLCC downsize	Y	Y	Y
9			R52	7.15K =>6.49K	Fixed OTP issue(BITS383003)	Y	Y	N